SSI Specification Micro Module Server

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Revision 1.0.1

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Revision History

The following table lists the revision schedule based on revision number and development stage of the product.

Revision	Project Document State	Date
0.10	First draft for internal review.	12/07/09
0.30	Draft proposal for external review.	12/23/09
0.80	Final content ready for partner review	4/10
0.85	Final content ready for member review	8/10
1.0	First public release	10/10
1.0.1	Release for public distribution	3/2012

Note: Not all revisions may be published.

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1 Introduction

1.1 Purpose

This *SSI Micro Module Server Specification* is intended to define a server board (aka Micro Module or µModule) form factor and connector. A micro server is an emerging server category that is generally described as a scale-out single socket, entry level, low cost, low power, improved density / efficiency and "good enough" performance server.

This specification encompasses board size, connector design, and connector pinout for two form factors relevant to the Micro Server segment. It also provides examples and guidelines for thermal design.

1.2 Scope

This revision of the Micro Module Specification is optimized to single socket server processor designs with four memory DIMMs and an integrated network controller.

1.3 Form Factors

Two form factors are proposed for the Micro Module Server

Top Access µModule – This form factor uses a card-edge connector on the long edge of the board for plugging µModules from the top of a chassis into a system baseboard.

Front Access µModule – This form factor uses a card-edge connector on the short edge of the board to allow for plugging µModules from the front of a chassis into a system backplane or midplane.

1.4 Audience

The primary audience for this specification is:

- Platform / System Architects
- Hardware Design Engineers
- Product Line Managers
- System Technologists and Planners
- Test and Validation Engineers
- Marketing Engineers and Planners

1.5 Specification Compliance

Products making the claim of compliance with this specification **shall** provide, at a minimum, all features defined as mandatory by the use of the keyword "**shall**". Such products **may** also provide recommended features associated with the keyword "**should**" and permitted features associated with the keyword "**may**".

1.6 Reference Documents

Note: Later revisions of the following specifications are allowed assuming backwards compatibility is maintained.

IEEE Std 802.3ap-2007 "Backplane Ethernet" standard.

IPMI – Intelligent Platform Management Interface Specification, v2.0 rev 1.0E3, February 16, 2006, Copyright © 2004, 2005, 2006 Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Inc., All rights reserved.

PCIe - PCI Express® Base Specification Revision 2.0, December 20, 2006, PCI-SIG®, all rights reserved.

PCIe - PCI Express® Card ElectroMechanical Specification Revision 2.0, April 11, 2007, PCI-SIG®, all rights reserved.

Serial ATA Specification, Revision 1.0a.

Universal Serial Bus Specification (USB), Revision 2.0.

1.7 Terms and Abbreviations

The following terms and acronyms are used in specific ways throughout this specification:

Table 1-1: Terms and Abbreviations

Term	Definition
BMC	Baseboard Management Controller. A management controller local to the Micro Module Server. A BMC is typically IPMI compliant.
CFM	Cubic Feet per Minute. A measure of volumetric airflow. One CFM is equivalent to 472 cubic centimeters per second.
Chassis	The mechanical enclosure that consists of the baseboard or midplane, Micro Module Servers, cooling devices, power supplies, hard disk drives, etc. The chassis provides the interface to boards and consists of the guide rails, alignment, handle interfaces, face plate mounting hardware, etc.
Component side	When used in reference to a PBA, the side on which the tallest electronic components such as the CPU and DIMMs would be mounted. Also called the Primary Side.
Guide Rail	May provide for the Micro Module Server board guidance feature in a slot.
HDD	Hard Disk Drive (magnetic)

Term	Definition
Intelligent Platform Management Bus (IPMB)	IPMB is an I^2C-based bus that provides a standardized interconnection between managed modules within a chassis. ftp://download.intel.com/design/servers/ipmi/ipmb1010ltd.pdf
Intelligent Platform Management Interface (IPMI)	IPMI v2.0 R1.0 specification defines a standardized, abstracted interface to the platform management subsystem of a computer system. ftp://download.intel.com/design/servers/ipmi/IPMIv2_0rev1_0.pdf
Interconnect Channel	An interconnect channel is comprised of two pairs of differential signals. One pair of differential signals for transmit and another pair of differential signals for receive.
Link	Network link representing either a single channel or aggregation of channels (example: KX4 using 4 channels would be a single Link). The term “Link” does not represent virtualized aggregation such as “teaming”.
LFM	Linear Feet per Minute. A measure of air velocity. One LFM is equivalent to 0.508 centimeters per second.
may	Indicates flexibility of choice with no implied preference.
Midplane	Equivalent to a system backplane. This is a PBA that provides the common electrical interface for a chassis in which server and interface boards plug into the front and rear of the chassis.
Module	A physically separate chassis component that may be independently replaceable (e.g., a µModule Server or cooling module) or attached to some other component (e.g., a baseboard).
Node	A self-contained compute server. In a system with several µModules in a large chassis, each µModule may be referred to as a node.
PBA	Printed board assembly. A printed board assembly is a printed circuit board that has all electronic components attached to it.
PCB	Printed circuit board without components attached.
PCIe	PCI Express®
SATA	Serial ATA (Advanced Technology Attachment). A storage interface for connecting host bus adapters to mass storage devices such as hard disk drives and optical drives
Secondary side	When used in reference to a PBA, the side normally reserved for making solder connections with through-hole components on the Component Side but on which low height electronic components may also be mounted.
SERDES	Serializer/Deserializer. In this case SERDES refers to the full duplex differential pair signaling specified by the IEEE 802.3ap backplane Ethernet specifications.
Shall	Indicates a mandatory requirement. Designers must implement such mandatory requirements to ensure interchangeability and to claim conformance with this specification. The use of **shall not** indicates an action or implementation that is prohibited.
Should	Indicates flexibility of choice with a strongly preferred implementation. The use of **should not** indicates flexibility of choice with a strong preference that the choice or implementation be avoided.
Slot	A slot defines the position of one Micro Module Server in a chassis.
SSD	A solid-state drive (SSD) is a data storage device that uses solid-state memory to store persistent data. Used in place of a hard disk drive.
U	Unit of vertical height defined in IEC 60297-1 rack, shelf, and chassis height increments. 1U=1.75 inches.

Term	Definition
USB	Universal Serial Bus
µModule	Micro Module Server defined by this specification
VR	Voltage Regulator. The µModule is supplied 12VDC on the connector and requires local voltage regulation to derive all logic voltages.

2 µModule Architecture

2.1 Micro Module Server Goals

The overall goal is to define a standard that will make it easier for the industry to build products with a defined board outline and connector interface, enabling lower costs and a reduced time-to-market. As such, the standard will provide flexible specification that maximizes design leverage while providing ample room for OEM/ODM differentiation.

Two form factors are defined, one targeted on top access, the other on front access.

2.1.1 High-level Strategic Goals

The following are the high-level strategic goals of the µModule specification:

- Common connector interface to maximize design re-use
- Flexibility to enable industry innovation and OEM value add
- Form factor that maximizes density at the lowest cost
- Enable multi-computer servers, lowering total cost of ownership
- Limit standard to the most basic compute elements and I/O
- Target single socket low power, “good enough” server CPU performance
- Leave system feature and mechanical implementation to OEMs i.e. fabric, storage topology, manageability, hot-plug, chassis size, module pitch etc.

2.1.2 High-level Technical Goals

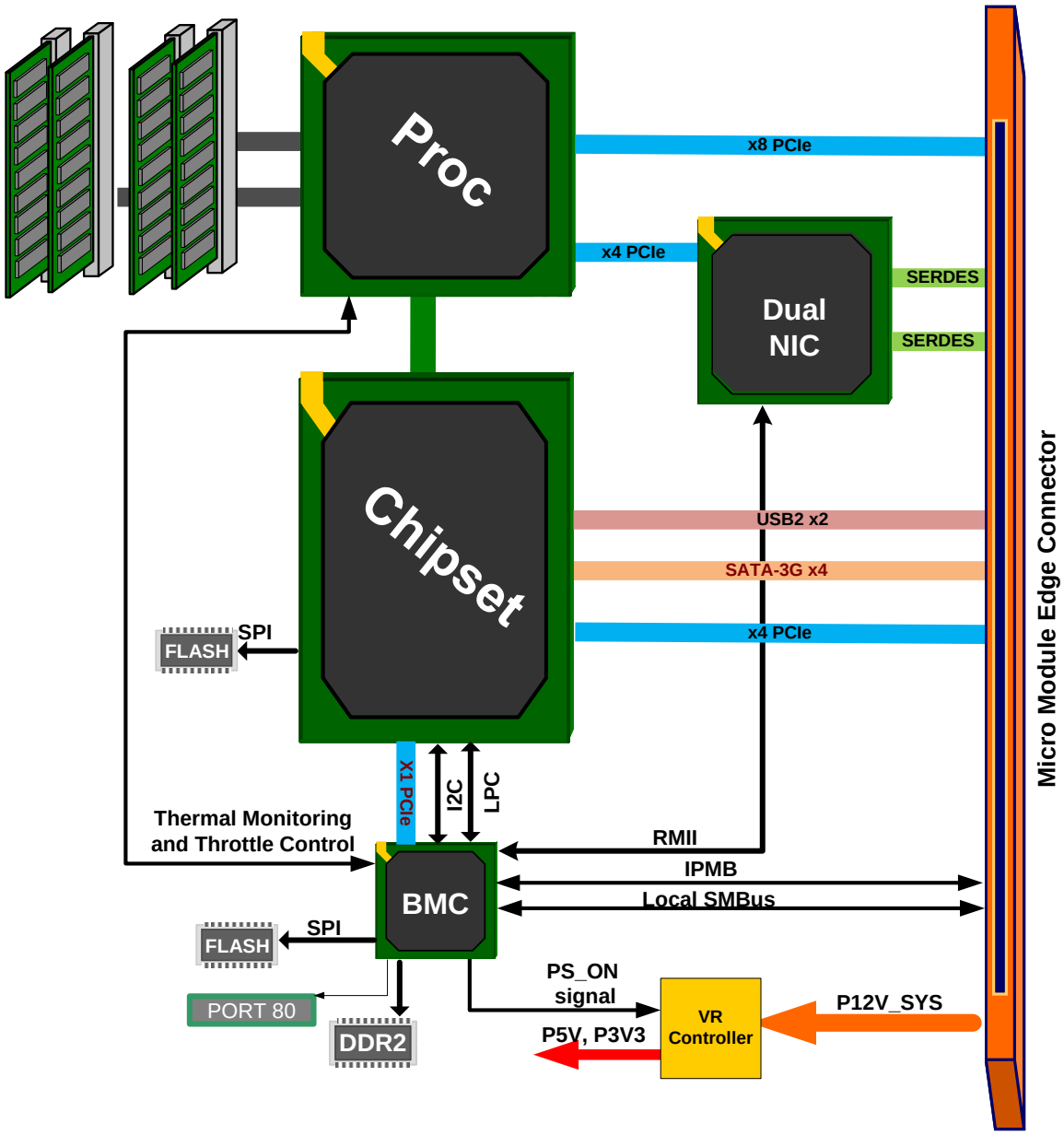
The following are the high-level technical goals of the µModule specification:

- Utilize proven high-volume connectors for low cost and TTM
- Enable rack mount chassis, <30” deep, with either front or rear I/O access
- Optimized density/scalability for 2-15kW racks
- Industry standard management interface
- Shared system resources for cost/power reduction
    - Power, cooling, management module
- Off-module I/O resources to enable small form factor and flexible system design
    - HDD/SDD, network switching & PHY, virtual KVM & media, USB connectors
- Two-tiered compatible connector approach
    - “Base” connector for basic computing elements
    - “Extended” connector for higher I/O capabilities and OEM/ODM differentiation

2.2 Typical µModule Functional Block Diagram

The Micro Module Server Specification defines the interface and form factor of the µModule. A typical block diagram of the system architecture is shown in Figure 2-1. Some implementations may have features on a faceplate which is beyond the scope of this specification.

Figure 2-1: Typical µModule Architecture



The key components of the µModule are:

- Single socket Processor and chipset

- System memory DIMMs
- Dual-channel Ethernet controller
- Baseboard Management Controller (BMC)
- Local voltage regulators (VR)
- Local Flash memory for BIOS & BMC firmware
- Debug support logic

2.3 Power Envelope

Although the maximum power for each form factor is defined, the power consumption of the system containing a µModule is not constrained by this specification. Thermal design of the system is the responsibility of the OEM.

2.4 µModule Connector Signal Groups

The µModule's connector signals are categorized into functional groups. Three groups are required while the others are optional. All signal locations **shall** be used only for the functions specified; they **shall not** be repurposed. See sections 3.2.1 and 4.2.1 for a graphical overview of the connector signal groups for the top access and front access µModules.

2.4.1 12V Power

Only 12V is delivered to the µModule through the baseboard or backplane connector. All main power rails **shall** be derived from the 12V rail.

2.4.2 Power Control

PRSNT0# and PRSNT1# are for µModule card presence detect. One present detect pin (with short edge finger contact) at each end of the base connector guarantees that at least one of the present detect pins is last-mate/first-break. This function can be used to enable hot-plug operations on the µModule by enabling/disabling power rails during plug/unplug operation. The PRSNT# signals are connected on the µModule. The system baseboard provides a pull-up resistor on one of the PRSNT# pins and grounds the other pin as shown in section 3.2 of *PCI Express® Base Specification Revision 2.0*

Note that the PRSNT# pins are not located at the same positions as on standard PCI Express connectors, and that CAD symbols must be modified to place the contacts with short pads at the correct pin positions as defined by this specification.

PWR_BTN# is an (active low) input indicating that a power button has been depressed to request a change to the µModule power state. This signal can also be asserted by a system management controller to control the power state of the µModule.

2.4.3 SSI Reserved Pins

SSI reserved pins on the connector definition are intended for future use. Systems **shall not** use the reserved pins for proprietary use. These pins **shall** remain unconnected.

2.4.4 SATA

The Micro Module Server supports up to four (4) SATA mass storage devices as defined by the Serial ATA Specification, Revision 1.0a. The base connector supports two (2) SATA devices, and the reference extended connector supports an additional two (2) SATA devices.

The directions of the high-speed signals are defined as "µModule"-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule's SATA controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule's SATA controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the SATA device(s) in the system.

2.4.5 3.3V Out

A 3.3V output pin is defined to provide power for functions directly related to a module. For example, SATA signals may require a re-driver located off the module which may be powered by this 1A source. Another possible use is to illuminate a power LED located off the module. This pin also provides indication that the power rails on the µModule are turned on, which may be used to turn on external voltage regulators for devices associated with this µModule (e.g. a PCIe device).

2.4.6 Identify

Two signals are provided to help identify a specific module in a system. The ID Button signal is an input that when active, causes the µModule to illuminate an ID LED. The ID LED signal is an output that provides the state of the module's ID LED to the backplane.

2.4.7 Slot ID

SLOT_ID_(5:0) provide strapping to the µModule to allow for uniquely identifying the physical slot in the system. These strapping pins should be routed to the µModule BMC or other management resources to provide unique system level management addressing.

The choice on how to physically number the slots in a system is system design responsibility.

2.4.8 I2C Management

There are two I2C buses on the connector for management.

IPMB_CLK and IPMB_DAT is an IPMI compliant management bus connecting a chassis or system level management entity to the Baseboard Management Controller (BMC) on the µModule.

SMBus_CLK and SMBus_DAT provide for a System Management Bus (SMBus) used for communication with devices under control of the µModule but physically located elsewhere in the system. Other devices might include temperature, fan or voltage sensors, a hot-swap controller, or PCIe add-in cards.

2.4.9 SERDES

This group provides for two network interconnects for the SSI Micro Module Server through a backplane SERDES interface. The basic parameters for the signals are defined in the IEEE Std. 802.3ap-2007 “Backplane Ethernet” standard.

The SERDES signal group, if used, **shall** support one of the following standards:

- IEEE Std 802.3ap-2007 “Backplane Ethernet” standard 1000BASE-KX for 1Gb Ethernet support.
- IEEE Std 802.3ap-2007 “Backplane Ethernet” standard 10GBASE-KR for 10Gb Ethernet support.

The directions of the high-speed signals are defined as “µModule”-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule’s Ethernet controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule’s Ethernet controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the switch module or PHY interface in the system.

Two LED signals are outputs associated with the network ports: ACT_LED_A# and ACT_LED_B# are (active low) LED indicator signals for Link Activity. These signals indicate activity on each of the SERDES Ethernet links controlled by µModule. Note: these signals are only present on the top access µModule connector. Activity LEDs for the front access µModule may be present on the module faceplate.

2.4.10 Management LAN

The management LAN group is for a dedicated management LAN. This LAN is a 100BASE-TX, point-to-point, full duplex interconnect.

The directions of the high-speed signals are defined as “µModule”-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule’s Ethernet controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule’s Ethernet controller. It is the responsibility of the system designer to properly connect the transmit pins from the µModule to the receive pins on the switch module or PHY interface in the system.

For backplane applications, it is common practice to use capacitive AC coupling verses magnetics. To do so typically requires Auto-Negotiation and Auto

MDI/MDIX to be disabled. Some PHYs may not support capacitive coupling. Refer to the PHYs manufacturer documentation for implementation details.

An LED signal is associated with the management LAN: MNGT_ACT_LED# is an (active low) LED indicator output signal for the Management LAN Link Activity. This signal indicates activity on the management Ethernet links controlled by µModule. Note: this signal is only present on the top access µModule connector. An activity LED for the front access µModule may be present on the module faceplate.

2.4.11 PCI Express®

The PCI Express® signals conform to *PCI Express® Base Specification Revision 2.0*. The x8 lanes on the top access µModule base connector can be bifurcated into two x4 lane segments using the two available clock pairs (PE_CLK_0 and PE_CLK_1). This is allowed if the x4 lanes on the extended connector (optional reference pinout) are not used. The x4 lanes on the extended connector are available for a secondary device in addition to the x8 lanes on the base connector. Only two PCIe end segments are supported from both the base connector and the extended connector, since there are two available clock pairs.

- The directions of the high-speed signals are defined as “µModule”-centric. The receiver differential pair of the connector **shall** be connected to the PCI Express Receiver differential pair of the µModule controller, and to the PCI Express Transmitter differential pair on PCI Express device off the µModule. The transmitter differential pair of the connector **shall** be connected to the PCI Express Transmitter differential pair on the µModule PCI Express controller, and to the PCI Express Receiver differential pair on PCI Express device off the µModule.
- The “P” and “N” connections **may** be reversed to simplify PCB trace routing and minimize vias if needed. All PCI-Express Receivers incorporate automatic Lane Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each Lane. Refer to Section 4.2.4 of the *PCI Express Base Specification, Revision 2.0*.
- Support for PCI Express Lane Reversal is optional on the µModule.

Note: Conformance to the PCIe specification and other open standards does not imply that erratum does not exist with the control chipsets.

2.4.12 USB

The top access µModule supports up to two USB devices as defined by the Universal Serial Bus Specification (USB), Revision 2.0.

The directions of the high-speed signals are defined as “µModule”-centric. As defined by the µModule interface connector, the transmit pairs on the connector **shall** connect to the transmit pins on the µModule’s USB controller. Similarly, the receive pins on the connector **shall** connect to the receive pins on the µModule’s USB controller. It is the responsibility of the system designer to

properly connect the transmit pins from the µModule to the receive pins on the USB device(s) in the system.

2.4.13 OEM / Future Use

This group is left undefined in the specification and may be used for OEM specific functions. This group may also be defined in future revisions of the specification. Feedback from µModule OEMs on features useful for the base connectors may be incorporated onto these pins in the future.

2.4.14 OEM Defined

The extended connector contains pins left up to the OEM to define. Optional reference pinouts for the top access and front access µModules are provided for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

2.5 µModule Connector Signal Definition

Table 2-1: µModule Connector Signal Definitions

Signal Name	Signal Description	Signal Group
12V	12VDC Power Supply Pins	12V Power
3.3V_OUT	3.3V Output (1A source)	3.3V Out
ACT_LED_A#	NIC Activity LED (active low) for SERDES A	SERDES
ACT_LED_B#	NIC Activity LED (active low) for SERDES B	SERDES
GND	Ground Pins	Ground
ID_BTN#	ID button pressed Input (active low)	Identify
ID_LED#	Module ID illuminated output (active low)	Identify
IPMB_CLK	IPMB Bus Serial Clock	I2C Management
IPMB_DAT	IPMB Bus Serial Data	I2C Management
MNGT_ACT_LED#	Management NIC Activity LED (active low)	Management LAN
MNGT_RX_DN	RX- of Mngt LAN	Management LAN
MNGT_RX_DP	RX+ of Mngt LAN	Management LAN
MNGT_TX_DN	TX- of Mngt LAN	Management LAN
MNGT_TX_DP	TX+ of Mngt LAN	Management LAN
OEM Defined	Defined by OEM	OEM Defined
OEM/Future Use	Defined by OEM / May be used in future	OEM/Future Use
PCIE_PERST#	PCIe Fundamental Reset output	PCI Express
PCIE_WAKE#	PCIe Wake# input	PCI Express
PE_A_RX_0_DN	RX- of Base PCIe Lane 0	PCI Express
PE_A_RX_0_DP	RX+ of Base PCIe Lane 0	PCI Express
PE_A_RX_1_DN	RX- of Base PCIe Lane 1	PCI Express
PE_A_RX_1_DP	RX+ of Base PCIe Lane 1	PCI Express
PE_A_RX_2_DN	RX- of Base PCIe Lane 2	PCI Express

PE_A_RX_2_DP	RX+ of Base PCIe Lane 2	PCI Express
PE_A_RX_3_DN	RX- of Base PCIe Lane 3	PCI Express
PE_A_RX_3_DP	RX+ of Base PCIe Lane 3	PCI Express
PE_A_RX_4_DN	RX- of Base PCIe Lane 4	PCI Express
PE_A_RX_4_DP	RX+ of Base PCIe Lane 4	PCI Express
PE_A_RX_5_DN	RX- of Base PCIe Lane 5	PCI Express
PE_A_RX_5_DP	RX+ of Base PCIe Lane 5	PCI Express
PE_A_RX_6_DN	RX- of Base PCIe Lane 6	PCI Express
PE_A_RX_6_DP	RX+ of Base PCIe Lane 6	PCI Express
PE_A_RX_7_DN	RX- of Base PCIe Lane 7	PCI Express
PE_A_RX_7_DP	RX+ of Base PCIe Lane 7	PCI Express
PE_A_TX_0_DN	TX- of Base PCIe Lane 0	PCI Express
PE_A_TX_0_DP	TX+ of Base PCIe Lane 0	PCI Express
PE_A_TX_1_DN	TX- of Base PCIe Lane 1	PCI Express
PE_A_TX_1_DP	TX+ of Base PCIe Lane 1	PCI Express
PE_A_TX_2_DN	TX- of Base PCIe Lane 2	PCI Express
PE_A_TX_2_DP	TX+ of Base PCIe Lane 2	PCI Express
PE_A_TX_3_DN	TX- of Base PCIe Lane 3	PCI Express
PE_A_TX_3_DP	TX+ of Base PCIe Lane 3	PCI Express
PE_A_TX_4_DN	TX- of Base PCIe Lane 4	PCI Express
PE_A_TX_4_DP	TX+ of Base PCIe Lane 4	PCI Express
PE_A_TX_5_DN	TX- of Base PCIe Lane 5	PCI Express
PE_A_TX_5_DP	TX+ of Base PCIe Lane 5	PCI Express
PE_A_TX_6_DN	TX- of Base PCIe Lane 6	PCI Express
PE_A_TX_6_DP	TX+ of Base PCIe Lane 6	PCI Express
PE_A_TX_7_DN	TX- of Base PCIe Lane 7	PCI Express
PE_A_TX_7_DP	TX+ of Base PCIe Lane 7	PCI Express
PE_B_RX_0_DN	RX- of Extended PCIe Lane 0	PCI Express
PE_B_RX_0_DP	RX+ of Extended PCIe Lane 0	PCI Express
PE_B_RX_1_DN	RX- of Extended PCIe Lane 1	PCI Express
PE_B_RX_1_DP	RX+ of Extended PCIe Lane 1	PCI Express
PE_B_RX_2_DN	RX- of Extended PCIe Lane 2	PCI Express
PE_B_RX_2_DP	RX+ of Extended PCIe Lane 2	PCI Express
PE_B_RX_3_DN	RX- of Extended PCIe Lane 3	PCI Express
PE_B_RX_3_DP	RX+ of Extended PCIe Lane 3	PCI Express
PE_B_TX_0_DN	TX- of Extended PCIe Lane 0	PCI Express
PE_B_TX_0_DP	TX+ of Extended PCIe Lane 0	PCI Express
PE_B_TX_1_DN	TX- of Extended PCIe Lane 1	PCI Express
PE_B_TX_1_DP	TX+ of Extended PCIe Lane 1	PCI Express
PE_B_TX_2_DN	TX- of Extended PCIe Lane 2	PCI Express
PE_B_TX_2_DP	TX+ of Extended PCIe Lane 2	PCI Express
PE_B_TX_3_DN	TX- of Extended PCIe Lane 3	PCI Express
PE_B_TX_3_DP	TX+ of Extended PCIe Lane 3	PCI Express
PE_CLK_1_DN	CLK- of PCIe Clock 1	PCI Express
PE_CLK_1_DP	CLK+ of PCIe Clock 1	PCI Express
PE_CLK_2_DN	CLK- of PCIe Clock 2	PCI Express

PE_CLK_2_DP	CLK+ of PCIe Clock 2	PCI Express
PRSNT0#	uModule Present 0 (active low, short pin)	Power Control
PRSNT1#	uModule Present 1 (active low, short pin)	Power Control
PWR_BTN#	Power Button Input (active low)	Power Control
RSVD	Reserved for future use. Do not use.	SSI Reserved
SATA_A_RX_DN	RX- of SATA Channel A	SATA
SATA_A_RX_DP	RX+ of SATA Channel A	SATA
SATA_A_TX_DN	TX- of SATA Channel A	SATA
SATA_A_TX_DP	TX+ of SATA Channel A	SATA
SATA_B_RX_DN	RX- of SATA Channel B	SATA
SATA_B_RX_DP	RX+ of SATA Channel B	SATA
SATA_B_TX_DN	TX- of SATA Channel B	SATA
SATA_B_TX_DP	TX+ of SATA Channel B	SATA
SATA_C_RX_DN	RX- of SATA Channel C	SATA
SATA_C_RX_DP	RX+ of SATA Channel C	SATA
SATA_C_TX_DN	TX- of SATA Channel C	SATA
SATA_C_TX_DP	TX+ of SATA Channel C	SATA
SATA_D_RX_DN	RX- of SATA Channel D	SATA
SATA_D_RX_DP	RX+ of SATA Channel D	SATA
SATA_D_TX_DN	TX- of SATA Channel D	SATA
SATA_D_TX_DP	TX+ of SATA Channel D	SATA
SerDes_A_RX_DN	Rx- of SerDes Channel A	SERDES
SerDes_A_RX_DP	Rx+ of SerDes Channel A	SERDES
SerDes_A_TX_DN	Tx- of SerDes Channel A	SERDES
SerDes_A_TX_DP	Tx+ of SerDes Channel A	SERDES
SerDes_B_RX_DN	Rx- of SerDes Channel B	SERDES
SerDes_B_RX_DP	Rx+ of SerDes Channel B	SERDES
SerDes_B_TX_DN	Tx- of SerDes Channel B	SERDES
SerDes_B_TX_DP	Tx+ of SerDes Channel B	SERDES
SLOT_ID_0	uModule ID Address 0	Slot ID
SLOT_ID_1	uModule ID Address 1	Slot ID
SLOT_ID_2	uModule ID Address 2	Slot ID
SLOT_ID_3	uModule ID Address 3	Slot ID
SLOT_ID_4	uModule ID Address 4	Slot ID
SLOT_ID_5	uModule ID Address 5	Slot ID
SMBus_CLK	Local SMBus Serial Clock	I2C Management
SMBus_DAT	Local SMBus Serial Data	I2C Management
USB_A_DN	USB Port A Data+	USB
USB_A_DP	USB Port A Data-	USB
USB_A_OC#	USB Port A Over Current	USB
USB_B_DN	USB Port B Data+	USB
USB_B_DP	USB Port B Data-	USB
USB_B_OC#	USB Port B Over Current	USB

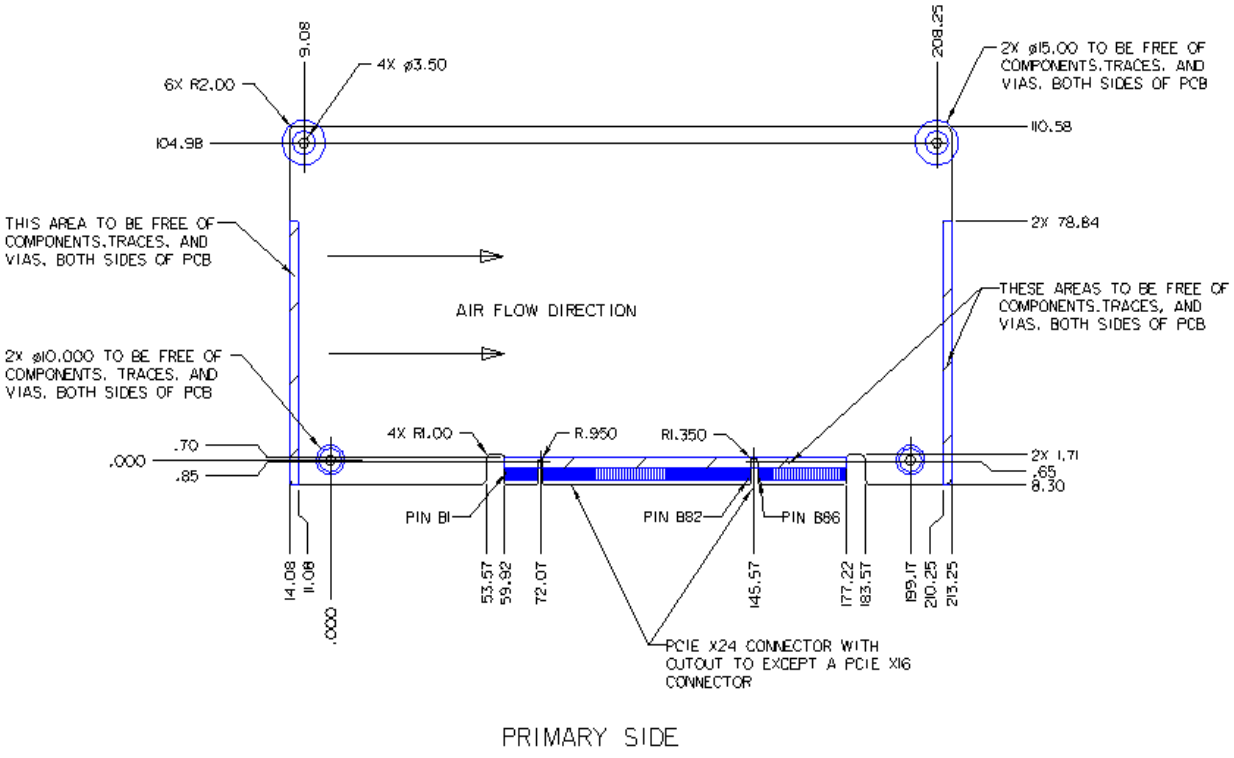
3 Top Access µModule

3.1 Board Outline and Keepouts

The top access µModule PBA dimension shall **be 4.680 inches x 8.95 inches, as shown in**

Figure 3-1: Top Access µModule PBA Dimensions. Figure 3-2 illustrates a physical view of a typical µModule PBA.

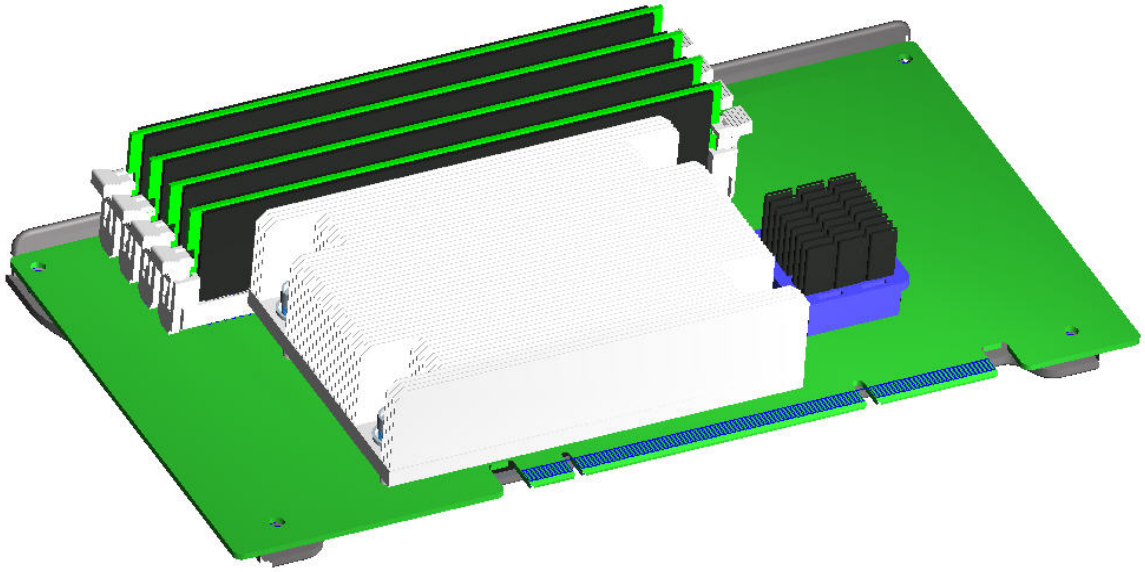
Figure 3-1: Top Access µModule PBA Dimensions



Note: Dimensions in mm unless otherwise stated.

Note: If unused, gold plating may be omitted on the extended connector (pins 86-115), or the physical edge fingers may be removed. The notch from 177mm to 183mm may not be removed so that the module can be inserted in a x24 extended connector.

Figure 3-2: Isometric View of Typical Top Access µModule



3.1.1 PBA Thickness

The µModule PBA thickness is specified at 0.062" [1.57mm] ± 0.005". [0.13mm].

3.1.2 Primary Side Component Height

The *primary* side of the µModule contains the processor and memory. The maximum component height is dependent on the system design and the desired module-to-module pitch within the system.

For designs using standard DIMMs (1U enabled components), the recommended maximum component height is 1.378" [35.00mm]

For designs using Very Low Profile (VLP) DIMMs, the recommended maximum component height is 0.897" [22.78mm].

3.1.3 Secondary Side Component Height

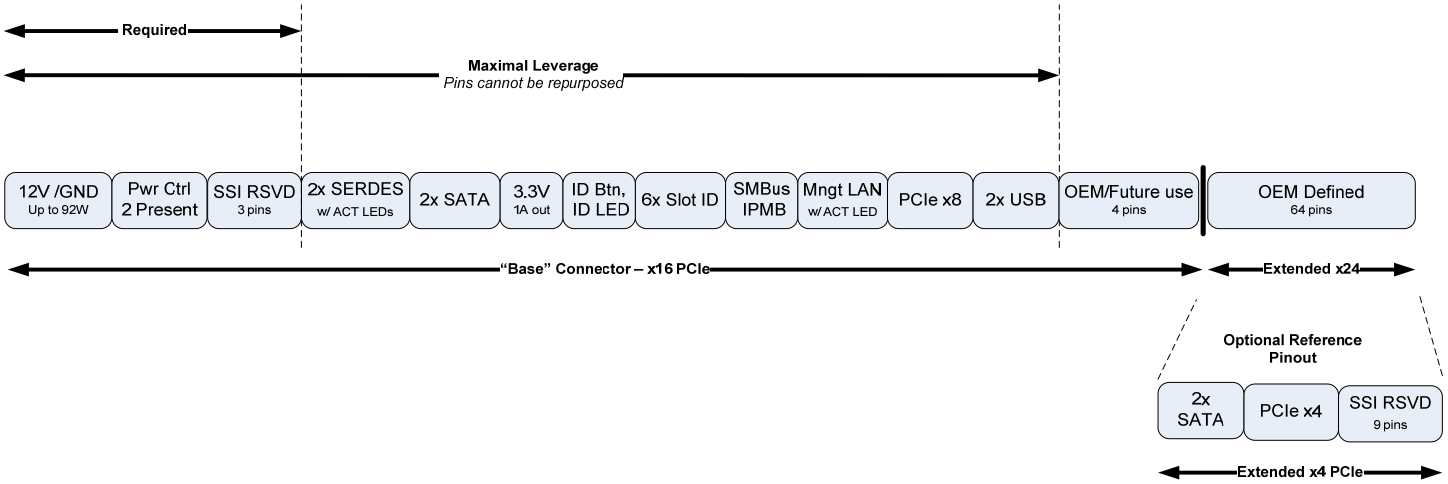
The *secondary* side of the µModule PBA is the side opposite the processor and memory. The **maximum** component height **shall** not exceed 0.125" [3.18mm].

3.2 Top Access µModule Connector Specification

3.2.1 Connector Overview

Figure 3-3 below provides a logical overview of the top access µModule connector.

Figure 3-3: Top Access µModule Connector Diagram



The top access µModule uses an edge finger connector derived from the PCI Express Specifications. There are two sections to the connector, base and extended.

The "Base" connector **shall** be present for all µModules and has the same mechanical definition as the 164 pin, x16 PCIe connector defined by the PCIe specifications.

Within the Base section the following functions **shall** be implemented:

- 12V Power delivery to the µModule
- Power control
- Reserved (RSVD)

The remaining functions are optional for any given implementation, however it is recommended that all be implemented for maximum design leverage. Only pins designated OEM/Future use and OEM Defined may be repurposed for other functions.

- 2x SERDES links which can be routed to internal network switches or PHY interfaces
- 2x SATA ports to access external storage
- 3.3V out
- ID button and LED
- Slot IDs to uniquely identify each µModule in a system

- Two I2C busses. One for chassis level communication to the µModule via a standard IPMB. The second for µModule SMBus access of local resources that reside off the µModule.
- Dedicated Management LAN
- 8x lanes of standard PCIe 2.0, which can be operated as a x8 link or bifurcated in two links if the extended 4X lanes are not used. A maximum of two PCIe endpoints are supported.
- 2x USB 2.0 ports
- 4 pins for OEM specific functions or functions to be defined in a future revision

The "Extended" connector section **may** be present and provides for additional I/O needed in certain applications. This 60 pin extension pinout and function are left unspecified and may be defined by an OEM. The following functions provide a reference for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

- 2x SATA ports to access additional storage
- 4x lanes of standard PCIe 2.0 which can be operated as a x4 link or can be aggregated with a portion or all of the 8 lanes on the base connector. A maximum of two PCIe endpoints are permitted for the µModule with or without the extended connector.

A notch is present in the PCB to allow a µModule to plug into a base connector or an extended connector on the system baseboard. For a system utilizing the base connector only, standard high-volume x16 PCIe connectors are used on the baseboard, which provide for a very attractive cost point. Systems that require the higher feature set may use the extended connector using a x24 PCIe connector on the baseboard. Some systems **may** choose to have a mix of connectors on the baseboard to match their unique requirements.

3.2.2 Connector Pinout

Table 3-1 shows the µModule connector pinout and signal definitions.

Note: Green color indicates ground connection, and purple indicates 12V power connection. Blue colored pins are reserved, light blue pins are reserved for OEM/Future use, and grey pins are OEM Defined.

Pins B1-B82 and A1-A82 constitute the "base" Connector. The physical connector key and notch between pins 11 and 12 is defined by the PCIe specification.

Pins B86-B115 and A86-A115 constitute the "extended" Connector. The µModule has a notch on the card edge in place of pins 83-85 to allow plugging into a standard base connector. The extended connector does not have a physical key in this location. The pins are present and unused. The SSI Micro Module Server **may** provide an extended connector via edge finger contacts. If the extended connector is supported, the SSI Micro Module Server **may**

provide for the reference signals defined on the extended connector or **may** be used for other functions as defined by the OEM.

Table 3-1: Top Access Base Connector Pinout

Signal	Pin		Signal
12V	B1	A1	PRSNT0#
12V	B2	A2	GND
12V	B3	A3	GND
12V	B4	A4	GND
12V	B5	A5	GND
12V	B6	A6	GND
12V	B7	A7	GND
RSVD	B8	A8	GND
SLOT_ID_0	B9	A9	IPMB_CLK
SLOT_ID_1	B10	A10	IPMB_DATA
SLOT_ID_2	B11	A11	SLOT_ID_3
KEY	KEY		KEY
GND	B12	A12	PCIE_WAKE#
PE_A_TX_0_DP	B13	A13	PCIE_PERST#
PE_A_TX_0_DN	B14	A14	GND
GND	B15	A15	PE_A_RX_0_DP
GND	B16	A16	PE_A_RX_0_DN
PE_A_TX_1_DP	B17	A17	GND
PE_A_TX_1_DN	B18	A18	GND
GND	B19	A19	PE_A_RX_1_DP
GND	B20	A20	PE_A_RX_1_DN
PE_A_TX_2_DP	B21	A21	GND
PE_A_TX_2_DN	B22	A22	GND
GND	B23	A23	PE_A_RX_2_DP
GND	B24	A24	PE_A_RX_2_DN
PE_A_TX_3_DP	B25	A25	GND
PE_A_TX_3_DN	B26	A26	GND
GND	B27	A27	PE_A_RX_3_DP
GND	B28	A28	PE_A_RX_3_DN
PE_A_TX_4_DP	B29	A29	GND
PE_A_TX_4_DN	B30	A30	GND
GND	B31	A31	PE_A_RX_4_DP
GND	B32	A32	PE_A_RX_4_DN
PE_A_TX_5_DP	B33	A33	GND
PE_A_TX_5_DN	B34	A34	GND
GND	B35	A35	PE_A_RX_5_DP

GND	B36	A36	PE_A_RX_5_DN
PE_A_TX_6_DP	B37	A37	GND
PE_A_TX_6_DN	B38	A38	GND
GND	B39	A39	PE_A_RX_6_DP
GND	B40	A40	PE_A_RX_6_DN
PE_A_TX_7_DP	B41	A41	GND
PE_A_TX_7_DN	B42	A42	GND
GND	B43	A43	PE_A_RX_7_DP
GND	B44	A44	PE_A_RX_7_DN
PE_CLK_1_DP	B45	A45	GND
PE_CLK_1_DN	B46	A46	GND
GND	B47	A47	PE_CLK_2_DP
GND	B48	A48	PE_CLK_2_DN
OEM/Future Use	B49	A49	GND
PWR_BTN#	B50	A50	ID_BTN#
ID_LED#	B51	A51	OEM/Future Use
USB_A_OC#	B52	A52	OEM/Future Use
GND	B53	A53	OEM/Future Use
USB_A_DP	B54	A54	USB_B_OC#
USB_A_DN	B55	A55	GND
GND	B56	A56	USB_B_DP
GND	B57	A57	USB_B_DN
SATA_A_TX_DP	B58	A58	GND
SATA_A_TX_DN	B59	A59	GND
GND	B60	A60	SATA_A_RX_DP
GND	B61	A61	SATA_A_RX_DN
SATA_B_TX_DP	B62	A62	GND
SATA_B_TX_DN	B63	A63	GND
GND	B64	A64	SATA_B_RX_DP
GND	B65	A65	SATA_B_RX_DN
SerDes_A_TX_DP	B66	A66	GND
SerDes_A_TX_DN	B67	A67	GND
GND	B68	A68	SerDes_A_RX_DP
GND	B69	A69	SerDes_A_RX_DN
SerDes_B_TX_DP	B70	A70	GND
SerDes_B_TX_DN	B71	A71	GND
GND	B72	A72	SerDes_B_RX_DP
GND	B73	A73	SerDes_B_RX_DN
MNGT_TX_DP	B74	A74	GND
MNGT_TX_DN	B75	A75	MNGT_RX_DP
GND	B76	A76	MNGT_RX_DN

MNGT_ACT_LED#	B77	A77	GND
3.3V_OUT	B78	A78	RSVD
RSVD	B79	A79	SLOT_ID_4
ACT_LED_A#	B80	A80	SLOT_ID_5
ACT_LED_B#	B81	A81	SMBus_CLK
PRSNT1#	B82	A82	SMBus_DAT
	B83	A83	
KEY	B84	A84	**KEY**
	B85	A85	
OEM Defined	B86	A86	OEM Defined
OEM Defined	B87	A87	OEM Defined
OEM Defined	B88	A88	OEM Defined
OEM Defined	B89	A89	OEM Defined
OEM Defined	B90	A90	OEM Defined
OEM Defined	B91	A91	OEM Defined
OEM Defined	B92	A92	OEM Defined
OEM Defined	B93	A93	OEM Defined
OEM Defined	B94	A94	OEM Defined
OEM Defined	B95	A95	OEM Defined
OEM Defined	B96	A96	OEM Defined
OEM Defined	B97	A97	OEM Defined
OEM Defined	B98	A98	OEM Defined
OEM Defined	B99	A99	OEM Defined
OEM Defined	B100	A100	OEM Defined
OEM Defined	B101	A101	OEM Defined
OEM Defined	B102	A102	OEM Defined
OEM Defined	B103	A103	OEM Defined
OEM Defined	B104	A104	OEM Defined
OEM Defined	B105	A105	OEM Defined
OEM Defined	B106	A106	OEM Defined
OEM Defined	B107	A107	OEM Defined
OEM Defined	B108	A108	OEM Defined
OEM Defined	B109	A109	OEM Defined
OEM Defined	B110	A110	OEM Defined
OEM Defined	B111	A111	OEM Defined
OEM Defined	B112	A112	OEM Defined
OEM Defined	B113	A113	OEM Defined
OEM Defined	B114	A114	OEM Defined
OEM Defined	B115	A115	OEM Defined

Table 3-2 shows the reference pinout for the extended connector. This pinout provides a reference for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

Table 3-2: Top Access Extended Connector Reference Pinout

RSVD	B86	A86	GND
RSVD	B87	A87	SATA_C_RX_DP
GND	B88	A88	SATA_C_RX_DN
SATA_C_TX_DP	B89	A89	GND
SATA_C_TX_DN	B90	A90	GND
GND	B91	A91	SATA_D_RX_DP
GND	B92	A92	SATA_D_RX_DN
SATA_D_TX_DP	B93	A93	GND
SATA_D_TX_DN	B94	A94	GND
GND	B95	A95	PE_B_RX_0_DP
GND	B96	A96	PE_B_RX_0_DN
PE_B_TX_0_DP	B97	A97	GND
PE_B_TX_0_DN	B98	A98	GND
GND	B99	A99	PE_B_RX_1_DP
GND	B100	A100	PE_B_RX_1_DN
PE_B_TX_1_DP	B101	A101	GND
PE_B_TX_1_DN	B102	A102	GND
GND	B103	A103	PE_B_RX_2_DP
GND	B104	A104	PE_B_RX_2_DN
PE_B_TX_2_DP	B105	A105	GND
PE_B_TX_2_DN	B106	A106	GND
GND	B107	A107	PE_B_RX_3_DP
GND	B108	A108	PE_B_RX_3_DN
PE_B_TX_3_DP	B109	A109	GND
PE_B_TX_3_DN	B110	A110	RSVD
GND	B111	A111	RSVD
RSVD	B112	A112	RSVD
RSVD	B113	A113	RSVD
RSVD	B114	A114	RSVD
RSVD	B115	A115	RSVD

3.3 Top Access µModule Power Requirements

The top access µModule supports a 90W power envelope. All power to the module is provided through the 12V pins. The Module **shall** draw a maximum of 7.5A from the 12V rail.

There is a 3.3V OUT pin that a module may support. It shall provide 1A.

3.4 Connector Mechanical Specification

The top access µModule edge connector is modeled after the PCI Express connector specified in *PCI Express® Card ElectroMechanical Specification Revision 2.0.* The 164 edge fingers in the µModule base connector are specified the same as the x16 I/O Card in section 5.2 (Connector Interface Definitions) of that document. The extended connector drawing is provided by this document. A notch is present between the base connector edge fingers and the extended connector edge fingers to allow an extended finger µModule to plug into either a base or extended connector receptacle.

The gold edge finger contacts **shall** conform to the same specifications as the PCI Express specification. Two pins on the µModule are shortened contacts to provide last break / first mate functionality:

- PRSNT0# (pin A1)
- PRSNT1# (pin B82)

These two contacts **shall** conform to the same specification as pin A1 of the PCI Express specification.

3.4.1 Connector Receptacles

The top access µModule typically plugs into a horizontal baseboard. PCIe x16 connectors are standard in the industry and are available from multiple suppliers.

PCIe x24 connectors are not defined by the PCIe specification, but are available from multiple vendors. Two vendors which supply this connector are:

Molex p/n 87715-3908

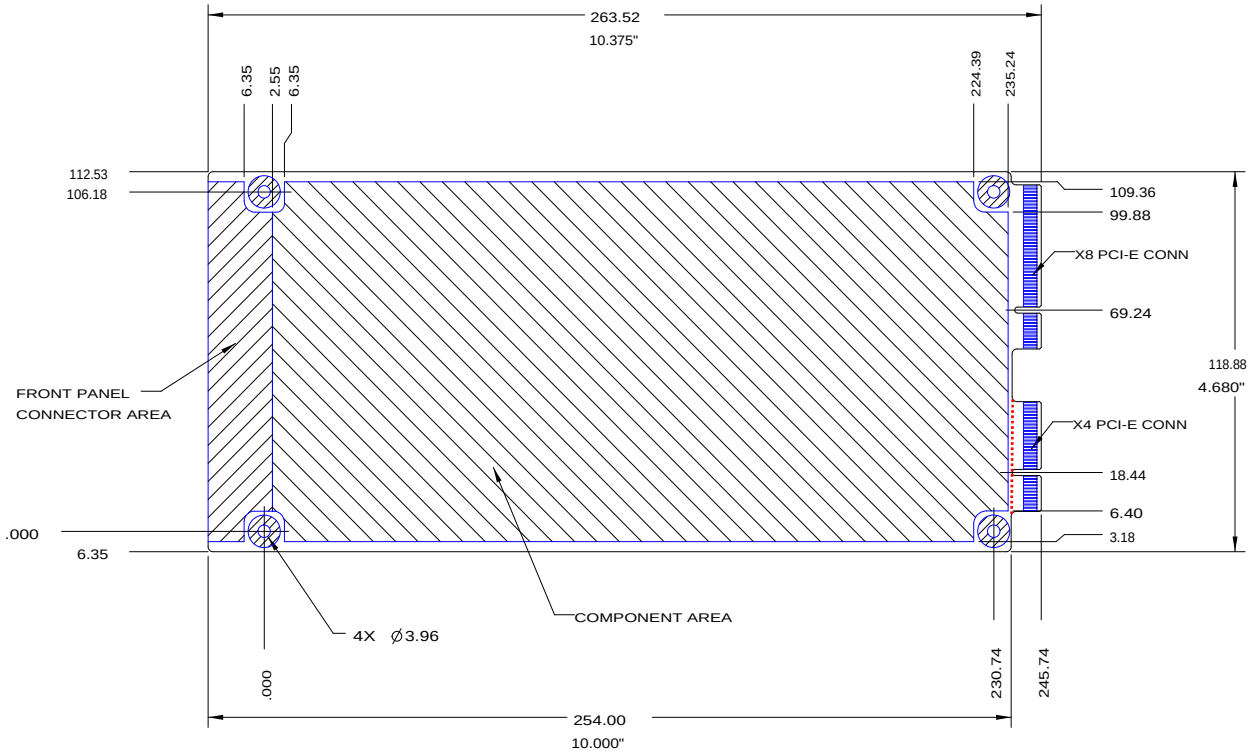
FCI p/n 10063960-10120TLF

4 Front Access µModule

4.1Board Outline and Keepouts

In order to facilitate plugging of one or several µModule servers in the front of a chassis, the following form factor is specified. A face plate, insertion / extraction lever, and limited I/O would typically be present on the front panel (left side on the drawing below). The Front Access µModule PBA dimension **shall be** 4.680 inches x 10.375 inches, as shown in Figure 4-1. Figure 4-2 shows an alternate version of the extended connector based on a PCIe x1 interface. Figure 4-3 represents a physical view of a typical µModule PBA.

Figure 4-1: Front Access µModule PBA Dimensions

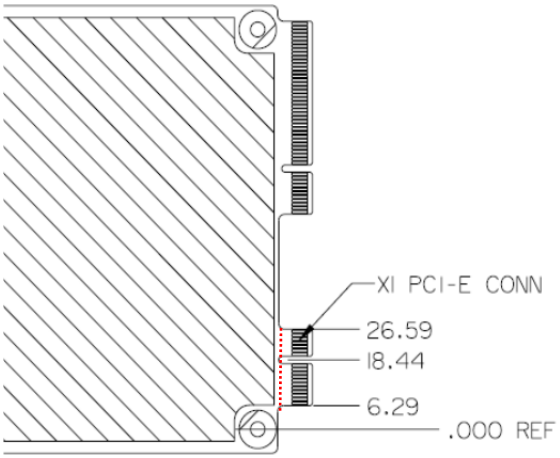


PRIMARY SIDE

Note: Dimensions in mm unless stated otherwise.

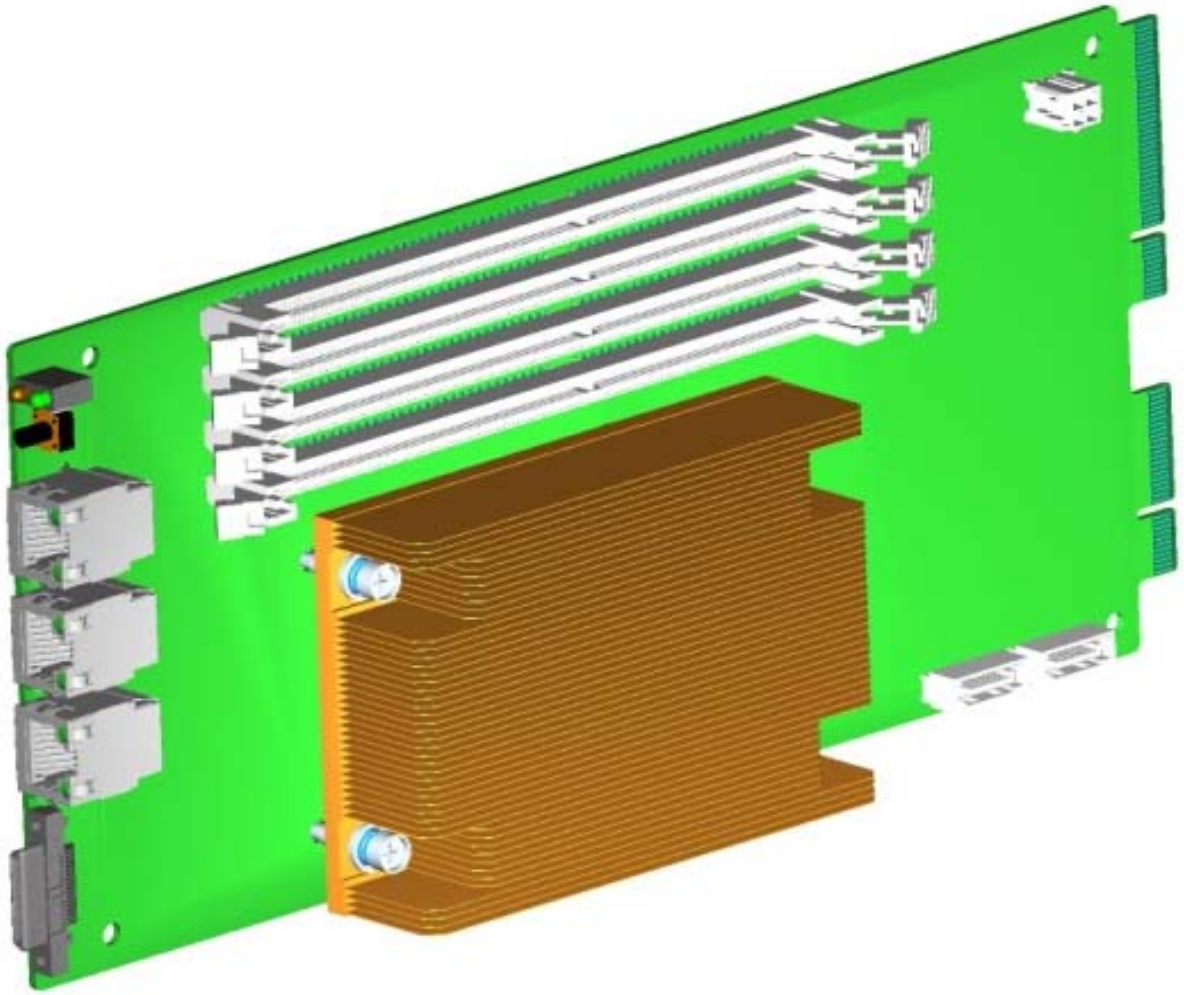
Note: The extended connector (x4 PCI-E) may be omitted. In this case the card edge aligns with the edge at the lower right corner (dotted line).

Figure 4-2: Front Access µModule: Alternative Extended Connector (x1)



Note: The extended connector may be omitted. In this case the card edge aligns with the edge at the lower right corner (dotted line).

Figure 4-3: Isometric View of Typical Front Access µModule



4.1.1 PBA Thickness

The µModule PBA thickness is specified at 0.062" [1.57mm] ± 0.005". [0.13mm].

4.1.2 Primary Side Component Height

The *primary* side of the µModule contains the processor and memory. The maximum component height is dependent on the system design and the desired module to module pitch within the system.

For designs using standard DIMMs (1U enabled components), the recommended maximum component height is 1.378" [35.00mm]

For designs using Very Low Profile (VLP) DIMMs, the recommended maximum component height is 0.897" [22.78mm].

4.1.3 Secondary Side Component Height

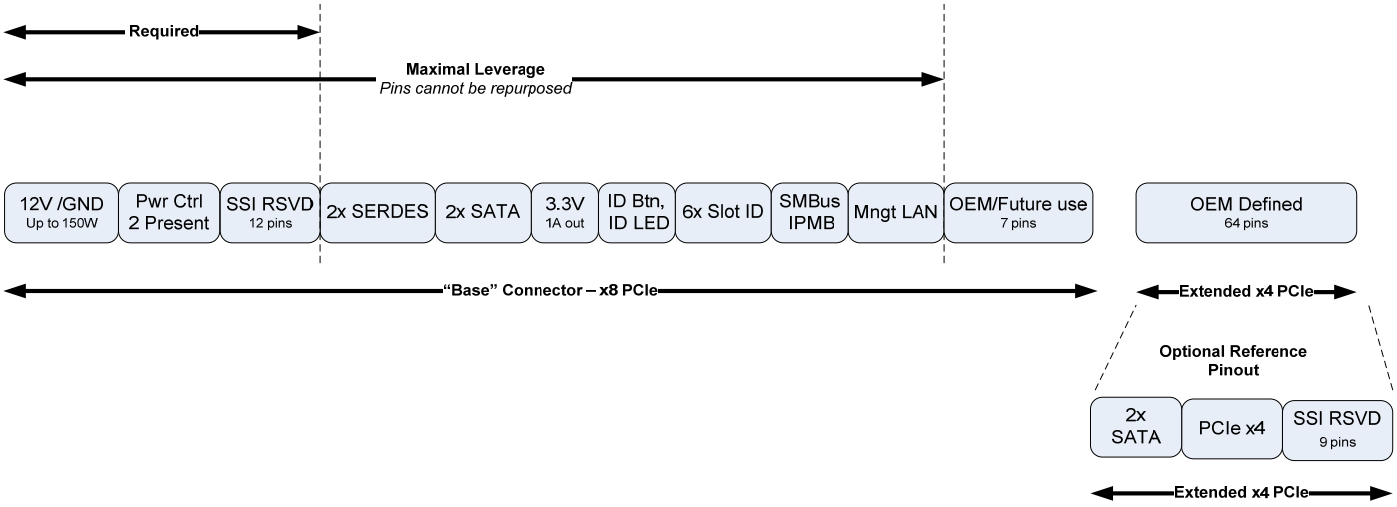
The *secondary* side of the µModule PBA is the side opposite the processor and memory. The **maximum** component height **shall** not exceed 0.125" [3.18mm].

4.2Front Access µModule Connector Specification

4.2.1 Connector Overview

Figure 4-4 below provides a logical overview of the front access µModule connector.

Figure 4-4: Front Access µModule Connector Diagram



The front access µModule uses an edge finger connector derived from the PCI Express Specifications. Two physical PCIe connectors may be used; a base (x8) connector and an extended (x4) connector. It is also permissible to use an alternative extended connector based on a PCIe x1 connector.

The "Base" connector **shall** be present for all µModules and has the same mechanical definition as the 98 pin x8 PCIe connector defined the PCIe specifications.

Within the Base section the following functions are required to be implemented as specific:

- 12V Power delivery
- Power control
- Reserved (RSVD) pins for future specification use

The remaining functions are optional for any given implementation however it is recommended that all be implemented for maximum design leverage. Only pins designated OEM/Future use and OEM Defined may be repurposed for other functions.

- Slot IDs to uniquely identify each µModule in a system
- Two I2C busses. One for chassis level communication to the µModule via a standard IPMB. The second for µModule SMBus access of local resources that reside off the µModule.
- 2x SATA ports to access external storage
- 2x SERDES links which can be routed to internal network switches or PHY interfaces
- 1x dedicated Mngt LAN
- 4 pins for OEM specific functions and functions to be defined in a future revision.

The “Extended” connector (x4) **may** be present and provides for additional I/O needed in certain applications. This 64 pin extension pinout and function are left unspecified and may be defined by an OEM. The following functions provide a reference for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

- 2x SATA ports to access additional storage
- 4x lanes of standard PCIe 2.0 which can be operated as a x4 link.

The alternative extended connector (x1) **may** be present and provides for additional I/O needed in certain applications. This 36 pin extension pinout and function are left unspecified and may be defined by an OEM.

4.2.2 Connector Pinout

Table 4-1 shows the Base connector pinout, and Table 4-2 shows the Extended connector pinout

Note: Green color indicates ground connection and purple indicates 12V power connection. Blue pins are reserved, light blue pins are reserved for OEM/Future use, and grey pins are OEM Defined.

Table 4-1: Front Access Base Connector Pinout

Signal	Pin		Signal
PRSNT1#	B49	A49	RSVD
SLOT_ID_0	B48	A48	SLOT_ID_4
SLOT_ID_1	B47	A47	SLOT_ID_5
SLOT_ID_2	B46	A46	GND
SLOT_ID_3	B45	A45	SerDes_A_RX_DP
GND	B44	A44	SerDes_A_RX_DN
SerDes_A_TX_DP	B43	A43	GND
SerDes_A_TX_DN	B42	A42	GND
GND	B41	A41	SerDes_B_RX_DP
GND	B40	A40	SerDes_B_RX_DN
SerDes_B_TX_DP	B39	A39	GND
SerDes_B_TX_DN	B38	A38	ID_BTN#
GND	B37	A37	PWR_BTN#
RSVD	B36	A36	ID_LED#
SMBus_CLK	B35	A35	OEM/Future Use
SMBus_DAT	B34	A34	RSVD
GND	B33	A33	IPMB_CLK
MNGT_TX_DP	B32	A32	IPMB_DATA
MNGT_TX_DN	B31	A31	GND
GND	B30	A30	MNGT_RX_DP
OEM/Future Use	B29	A29	MNGT_RX_DN
OEM/Future Use	B28	A28	GND
OEM/Future Use	B27	A27	OEM/Future Use
RSVD	B26	A26	OEM/Future Use
RSVD	B25	A25	OEM/Future Use
RSVD	B24	A24	RSVD
RSVD	B23	A23	RSVD
GND	B22	A22	3.3V_OUT
SATA_A_TX_DP	B21	A21	RSVD
SATA_A_TX_DN	B20	A20	GND
GND	B19	A19	SATA_A_RX_DP
GND	B18	A18	SATA_A_RX_DN
SATA_B_TX_DP	B17	A17	GND
SATA_B_TX_DN	B16	A16	GND
GND	B15	A15	SATA_B_RX_DP
RSVD	B14	A14	SATA_B_RX_DN

RSVD	B13	A13	GND
12V	B12	A12	PRSNT0#
KEY	KEY		KEY
12V	B11	A11	GND
12V	B10	A10	GND
2V	B9	A9	GND
12V	B8	A8	GND
12V	B6	A7	GND
12V	B6	A6	GND
12V	B5	A5	GND
12V	B4	A4	GND
12V	B3	A3	GND
12V	B2	A2	GND
12V	B1	A1	GND

Table 4-2 Front Access Extended Connector Pinout

Signal	Pin		Signal
OEM Defined	B32	A32	OEM Defined
OEM Defined	B31	A31	OEM Defined
OEM Defined	B30	A30	OEM Defined
OEM Defined	B29	A29	OEM Defined
OEM Defined	B28	A28	OEM Defined
OEM Defined	B27	A27	OEM Defined
OEM Defined	B26	A26	OEM Defined
OEM Defined	B25	A25	OEM Defined
OEM Defined	B24	A24	OEM Defined
OEM Defined	B23	A23	OEM Defined
OEM Defined	B22	A22	OEM Defined
OEM Defined	B21	A21	OEM Defined
OEM Defined	B20	A20	OEM Defined
OEM Defined	B19	A19	OEM Defined
OEM Defined	B18	A18	OEM Defined
OEM Defined	B17	A17	OEM Defined
OEM Defined	B16	A16	OEM Defined
OEM Defined	B15	A15	OEM Defined
OEM Defined	B14	A14	OEM Defined
OEM Defined	B13	A13	OEM Defined
OEM Defined	B12	A12	OEM Defined

KEY	KEY		KEY
OEM Defined	B11	A11	OEM Defined
OEM Defined	B10	A10	OEM Defined
OEM Defined	B9	A9	OEM Defined
OEM Defined	B8	A8	OEM Defined
OEM Defined	B6	A7	OEM Defined
OEM Defined	B6	A6	OEM Defined
OEM Defined	B5	A5	OEM Defined
OEM Defined	B4	A4	OEM Defined
OEM Defined	B3	A3	OEM Defined
OEM Defined	B2	A2	OEM Defined
OEM Defined	B1	A1	OEM Defined

Table 4-3 shows the reference pinout for the extended connector. This pinout provides a reference for OEMs and ODMs that would prefer to maximize design leverage across multiple board designs and system implementations.

Table 4-3: Front Access Extended Connector Reference Pinout

Signal	Pin		Signal
RSVD	B32	A32	RSVD
RSVD	B31	A31	GND
RSVD	B30	A30	PE_A_RX_3_DP
GND	B29	A29	PE_A_RX_3_DN
PE_A_TX_3_DP	B28	A28	GND
PE_A_TX_3_DN	B27	A27	GND
GND	B26	A26	PE_A_RX_2_DP
GND	B25	A25	PE_A_RX_2_DN
PE_A_TX_2_DP	B24	A24	GND
PE_A_TX_2_DN	B23	A23	GND
GND	B22	A22	PE_A_RX_1_DP
GND	B21	A21	PE_A_RX_1_DN
PE_A_TX_1_DP	B20	A20	GND
PE_A_TX_1_DN	B19	A19	GND
GND	B18	A18	PE_A_RX_0_DP
GND	B17	A17	PE_A_RX_0_DN
PE_A_TX_0_DP	B16	A16	GND
PE_A_TX_0_DN	B15	A15	GND
GND	B14	A14	PE_CLK_1_DP
PCIE_PERST#	B13	A13	PE_CLK_1_DN
PCIE_WAKE#	B12	A12	GND

KEY	KEY		KEY
RSVD	B11	A11	RSVD
GND	B10	A10	RSVD
SATA_C_TX_DP	B9	A9	GND
SATA_C_TX_DN	B8	A8	GND
GND	B6	A7	SATA_C_RX_DP
GND	B6	A6	SATA_C_RX_DN
SATA_D_TX_DP	B5	A5	GND
SATA_D_TX_DN	B4	A4	GND
GND	B3	A3	SATA_D_RX_DP
RSVD	B2	A2	SATA_D_RX_DN
RSVD	B1	A1	GND

4.3 Front Access µModule Power Requirements

The front access µModule supports a power envelope of 150W. All power to the module is provided through the 12V pins. The Module **shall** draw a maximum of 12.5A from the 12V rail.

There is a 3.3V OUT pin that a module may support. It shall provide 1A.

4.4 Connector Mechanical Specification

The front access µModule edge connectors are modeled after the PCI Express connector specified in *PCI Express® Card ElectroMechanical Specification Revision 2.0.* The 98 edge fingers in the µModule base connector are specified the same as the x8 I/O Card in section 5.2 (Connector Interface Definitions) of that document.

The 64 edge fingers in the µModule extended connector are specified the same as the x4 I/O Card in section 5.2 (Connector Interface Definitions) of that document.

The 36 edge fingers in the µModule alternative extended connector are specified the same as the x1 I/O Card in section 5.2 (Connector Interface Definitions) of that document.

The gold edge finger contacts **shall** conform to the same specifications as the PCI Express specification. Two pins on the µModule's base connector are shortened contacts to provide last break / first mate functionality:

- PRSNT0# (pin A12)
- PRSNT1# (pin B49)

These two contacts **shall** conform to the same specification as pin A1 of the PCI Express specification.

4.4.1 Connector Receptacles

The front access µModule typically plugs into a vertical backplane or midplane. PCIe x8, PCIe x4, and PCIe x1 connectors are standard in the industry and are available from multiple suppliers.

5 Product Regulations Compliance

The SSI Micro Module Server **shall** meet regulatory requirements as governed by specific country regulations.

