SSI Chassis Management Module (CMM) Specification

Specification

November 2010

Revision 1.0.2

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Revision History

The following table lists the revision schedule based on revision number and development stage of the product.

Revision	Project Document State	Date
1.0.0	Initial public release	9/18/2009
1.0.2	Bug updates: 273, 274, 304,	November 4, 2010

Note: Not all revisions may be published.

1 Introduction

1.1 Scope

This Chassis Management Module (CMM) Specification for the SSI Blade Standard defines a set of standard hardware and management interfaces for SSI-compliant blade server platforms.

It **shall** be noted that in redundant CMM configurations only CMM's that are of the same manufacturer or design **shall** be used in the same chassis. There are currently no plans to allow "mix and match" CMMs from different manufacturers or design in any redundant CMM configuration.

1.2 Purpose

The primary purpose of the SSI CMM specification is to:

- Promote interoperability across building blocks from multiple vendors.
- Maximize the use of common off-the-shelf components from the server industry, thereby reducing customer development costs and speeding time to market.
- Enable innovation and differentiation by allowing OEMs/ODMs to implement value-added differentiation, providing access to market share outside standard server designs.

1.3 Audience

The primary audiences for this specification are:

- Platform Architects
- System Architects
- Hardware Design Engineers
- Product Line Managers
- System Technologists and Planners
- Test and Validation Engineers
- Marketing Engineers and Planners

1.4 Specification Compliance

Products making the claim of compliance with this specification **shall** provide, at a minimum, all features defined as mandatory by the use of the keyword "**shall**". Such products may also provide recommended features associated with the keyword "should" and permitted features associated with the keyword "may".

System designs **shall** be based on using either “same manufacture” or “same design” CMMs in a redundant CMM configuration. The use of CMMs of different designs are NOT SUPPORTED in any SSI system design.

1.5 Reference Documents

- IPMI – Intelligent Platform Management Interface Specification, v2.0 rev 1.0E3, February 16, 2006, Copyright © 2004, 2005, 2006 Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Inc., All rights reserved.
- IPMI – Platform Management FRU Information Storage Definition, V1.0, Document revision 1.1, September 27, 1999 Copyright © 1998, 1999 Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Inc., All rights reserved.
- IPMI – Intelligent Platform Management Bus Communications Protocol Specification, V1.0, Document revision 1.0, November 15, 1999 Copyright © 1998, 1999 Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Inc., All rights reserved.
- I2C Bus Specification Version 2.1 or later from NXP Semiconductors: This can be found at: http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf
- SCSI Primary Commands – 2 (SPC-2) Revision 3 or later, ANSI/INCITS 351-2001.
- SCSI Reduced Block Commands (RBC), ANSI/INCITS 330-2000 [2006].
- Universal Serial Bus Mass Storage Class, Bulk-only Transport, Revision 1.0, Sept 31, 1999.
- PICMG 3.0 Revision 2.0 AdvancedTCA* Base Specification, March 18, 2005.
- SSI Compute Blade Specification.
- SSI Compute Blade Mezzanine Specification.
- SSI Midplane Electrical Specification.
- SSI Midplane Design Guide.
- IEEE Std. 802.3ap-2007 "Backplane Ethernet" standard.
- Advanced Configuration and Power Interface (ACPI) specification 2.0b.
- Extensible Firmware Interface (EFI) version 1.1.
- Unified Extensible Firmware Interface (UEFI) version 2.0.
- Trusted Computing Group (TCG) Trusted Platform Module (TPM) PC Client specifications version 1.2.
- Windows Hardware Error Architecture (WHEA) Platform Design Guide version 1.0.
- OEM Activation version 2.0 For Microsoft* Windows Vista* Operating systems.

- DMTF - System Management BIOS (SMBIOS) Reference specification 2.3.4.
- SD card specifications - http://www.sdcard.org/home/ [273]

1.6 Terms and Abbreviations

Table 1-1 lists terms and acronyms used in specific ways throughout this specification.

Table 1-1: Terms and Abbreviations

Term	Definition
ASHRAE	American Society of Heating, Refrigerating, and Air Conditioning Engineers.
Base Management Interface (BMI)	This is the IPMB-based management interface used by the Chassis Manager to communicate with the blade management controllers.
blade	This is a resource module that plugs into the blade chassis. A blade can provide many different types of resources to the chassis, including compute functions, storage capabilities, additional I/O interfaces and switching capabilities, and special purpose capabilities. A blade can be a single-wide module (assumed) or a double-wide module, occupying two adjacent slots in the chassis.
blade server	A system comprising a chassis, chassis resources (power, cooling, Chassis Manager), Compute Blades, and communication (switch) blades. The chassis may contain additional modules, such as storage.
bottom	When used in reference to a board, the end that would be on the bottom in a vertically oriented chassis.
CFM	Cubic Feet per Minute. A measure of volumetric airflow. One CFM is equivalent to 472 cubic centimeters per second.
chassis	The mechanical enclosure that consists of the mid-plane, front boards, cooling devices, power supplies, etc. The chassis provides the interface to boards, and it consists of the guide rails, alignment, handle interface, face plate mounting hardware, and mid-plane interface.
chassis ground	A safety ground and earth return that is connected to the chassis metal and available to all PBAs.
Chassis Management Module (CMM)	Dedicated intelligent chassis module that hosts the Chassis Manager functionality.
Chassis Manager (CM)	Set of logical functions for hardware management of the chassis. This may be implemented by one or more dedicated Chassis Management Modules or by one or more blade management controllers and/or payload processors.
cold start	Cold start is the time when blades receive the payload power for the first time.
component side 1	When used in reference to a PBA, the side on which the tallest electronic components would be mounted.
component side 2	When used in reference to a PBA, the side normally reserved for making solder connections with through-hole components on Component Side 1, but on which low-height electronic components may also be mounted.
creepage	Surface distance required between two electrical components.
face plate	The front-most element of a PBA, perpendicular to the PBA, that serves to mount connectors, indicators, controls, and mezzanines.
guide rail	Provides for the front board guidance feature in a slot.
handle	An item or part used to insert or extract blades into and out of chassis.

Term	Definition
Intelligent Platform Management Bus (IPMB)	IPMB is an I2C-based bus that provides a standardized interconnection between managed modules within a chassis. ftp://download.intel.com/design/servers/ipmi/ipmb1010ltd.pdf
Intelligent Platform Management Interface (IPMI)	IPMI v2.0 R1.0 specification defines a standardized, abstracted interface to the platform management subsystem of a computer system. ftp://download.intel.com/design/servers/ipmi/IPMIv2_0rev1_0.pdf
interconnect channel	An interconnect channel comprises two pairs of differential signals. One pair of differential signals for transmit and another pair of differential signals for receive.
LFM	Linear Feet per Minute. A measure of air velocity. One LFM is equivalent to 0.508 centimeters per second.
logic ground	Chassis-wide electrical net used on blades and mid-planes as a reference and return path for logic-level signals that are carried between boards.
managed module	Any component of the system that is addressable for management purposes via the specified management interconnect and protocol. A managed module is interfaced directly to the chassis BMI.
Management Controller	This is an intelligent, embedded microcontroller that provides management functionality for a blade or other chassis module.
may	Indicates flexibility of choice with no implied preference.
mezzanine	The mezzanine is a PBA that installs on a blade PBA horizontally. It provides additional functionality on the blade PBA and provides electrical interface between the blade PBA and the mid-plane PBA. Both the blade PBA and mezzanine PBA are contained inside the blade module.
mid-plane	Equivalent to a system backplane. This is a PBA that provides the common electrical interface for each blade in the chassis and on both the front and back of the PBA.
module	A physically separate chassis component which may be independently replaceable (e.g., a blade or cooling module) or attached to some other component (e.g., a mezzanine board).
open blade	A blade that conforms to the requirements defined by the Open Blade standard set of specifications.
out-of-band (OOB)	Communication between blades that does not need the host or payload to be powered on.
payload	The hardware on a blade that implements the main mission function of the blade. On a Compute Blade, this includes the main processors, memory, and I/O interfaces. The payload is powered separately from the blade management subsystem. Payload power is controlled by the blade management controller.
PBA	Printed board assembly. A printed circuit board that has all electronic components attached to it.
PCB	Printed circuit board without components attached.
Peak power	The maximum power a blade can draw for a very short period of time during a hot insertion, hot removal, or a cold start.
pitch line	Horizontal pitch line between slots.
shall	Indicates a mandatory requirement. Designers must implement such mandatory requirements to ensure interchangeability and to claim conformance with this specification. The use of **shall not** (in bold) indicates an action or implementation that is prohibited.

Term	Definition
should	Indicates flexibility of choice with a strongly preferred implementation. The use of **should not** (in bold) indicates flexibility of choice with a strong preference that the choice or implementation be avoided.
slot	A slot defines the position of one blade in a chassis.
top	When used in reference to a blade, the end which would be on top in a vertically oriented chassis.
U	Unit of vertical height defined in IEC 60297-1 rack, shelf, and chassis height increments. 1U=44.45 mm.
WDT	Watchdog timer.

2 CMM Architecture

2.1 CMM Overview

The SSI CMM Specification is provided for those system designers desiring to include a Chassis Management Module in their blade server system. The CMM comprises a printed circuit board assembly in a mechanical enclosure that plugs into the blade server system via interface connectors on the mid-plane board. The CMM provides remote management capability for system administrators to manage, provision, and configure the operation of the blade server system.

The CMM interfaces to the system via the interface connectors on the mid-plane, and communicates through multiple busses and protocols to the various modules in the system:

- I2C communication protocols such as PSMI and IPMB are used for low-level system modules, such as power supplies and fan modules.
- Both simple I2C and complex management via Ethernet 100 Mbps (TCP protocols) are used for more complex modules to support higher bandwidth functionality.
  Note that the High Speed switch specification requires that each instantiation of a high speed switch be located on a different logical I2C bus to prevent address interference.
- 100 Mbps Ethernet (TCP protocols) is used for I/O switch modules to support management functions.

The I2C bus **shall** be operated at 5V and be tolerant of 5V devices.

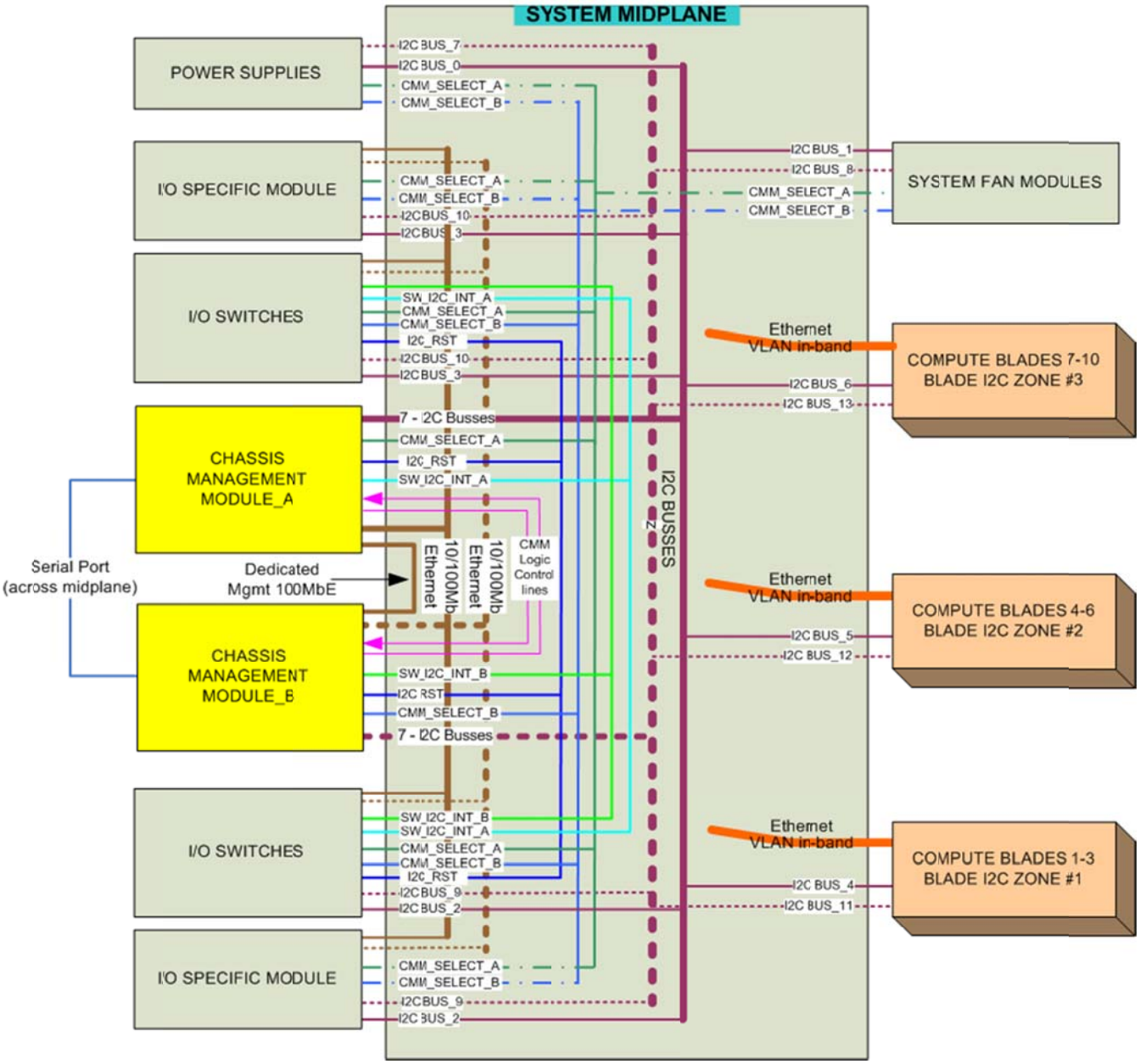
Figure 2-1 shows a block diagram of a typical system, with the management interconnections and bus types. Figures 2-2, 2-3, 2-4, and 2-5 show the details for a system design, breaking Figure 2-1 into multiple diagrams for clarity.

In a system with redundancy built into the system architecture, there will be two CMMs, with interconnections from each of the CMMs to each of the system modules. Some manner of software failover between the CMMs will allow them to decide which one is the primary system manager. The primary CMM in Figures 2-1, 2-2, and 2-3 is connected via solid lines, while the redundant CMM is indicated with dashed lines. See the diagram keys for clarification.

Note: In a redundant system, both CMMs **shall** be of the same manufacturer and design; i.e. they must be identical hardware and software.

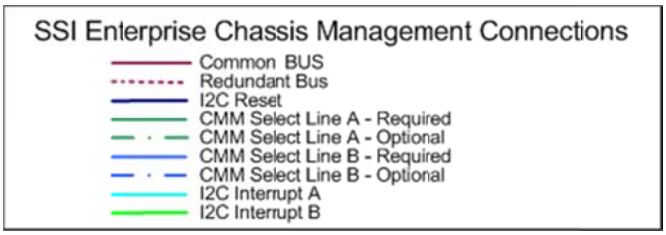
In addition to the normal management connections, there is a dedicated 100 MbE (minimum) connection and serial port connection between the two CMMs. These allow the CMMs to communicate separately from the rest of the system for determination of which module is the primary system manager.

Figure 2-1: Example of Redundant CMM Management Connection Diagram



Note: For description of blade management connections, see the SSI Compute Blade specification.

Fig 2-1 Key:



2.1.1 CMM Overview Signal Descriptions

The CMM signals are defined as follows:

- I2C busses consist of the I2C SDA and SCL (DATA and CLOCK) signals to each module. There are redundant I2C busses throughout the chassis, one from each of the CMMs. The CMM arbitration logic (described in section 3.2.4) determines the primary CMM and which I2C bus is enabled across the chassis. The busses **shall** conform to 5V logic levels, and be capable of working with 5V logic inputs, and each output driver will have a maximum sink capacity of 3mA.
- Ethernet signals consist of SERDES 100 Mbps Ethernet signals routed to the switch and I/O modules. There are two Ethernet connections into each of the modules.
- The Compute Blades use Ethernet management through a VLAN (virtual LAN) running within the normal blade GbE channels. There are two ports in the Compute Blade; they connect through the normal GbE switch channels to the CMM.
- I2C reset lines (I2C_RESET_N) are used by the CMMs to reset the I2C controllers in all of the switch modules. If system developers determine they want to reset other I2C controllers in other modules of the chassis, they will have to connect these lines accordingly. The minimum system requirement is to have the switches connected as specified by the SSI Switch Base Specification. The I2C_RESET_N lines are 5V logic level (active low, level sensitive) signals. The output strength of the CMM driver on these lines should sink a minimum of 3mA.
  NOTE: Depending upon the system design and the loading on these lines, a logic buffer may be needed on the midplane to assure keeping within the loading of the CMM output driver.
- Switch I2C interrupt lines (SW_I2C_INT_A/B) are signals from the switches to the CMMs that allow the switch modules to tell the CMM to read the status of the switch.
- CMM select lines (CMM_SELECT_A/B_N) are the select lines coming from either CMM A, or CMM B used by the various system modules to determine the primary CMM for I2C bus determination. A LOW on this signal for only one of the lines causes the various system modules to select that I2C bus from the module input. Should both lines be either high or low (logic level), the modules are to disconnect from the I2C bus. Refer to figure 2-3.
  The logic levels for this signal **shall** be 5V logic signals, with buffer drive strength of 3mA.
  NOTE: An INVERTING logic buffer is required on the midplane to assure the proper logic signal sense to the SSI Switch select inputs. See the SSI Midplane design guide for details.
- CMM Failover logic control lines, (CMM_LOGIC_CONTROL_IN/OUT) between the CMMs are used by the arbitration logic in the two CMMs to determine which I2C bus is active. Refer to Figure 2-5. These **shall** be LVTTL logic compatible signals.

Figure 2-2: Redundant CMM Management I2C Connection Diagram

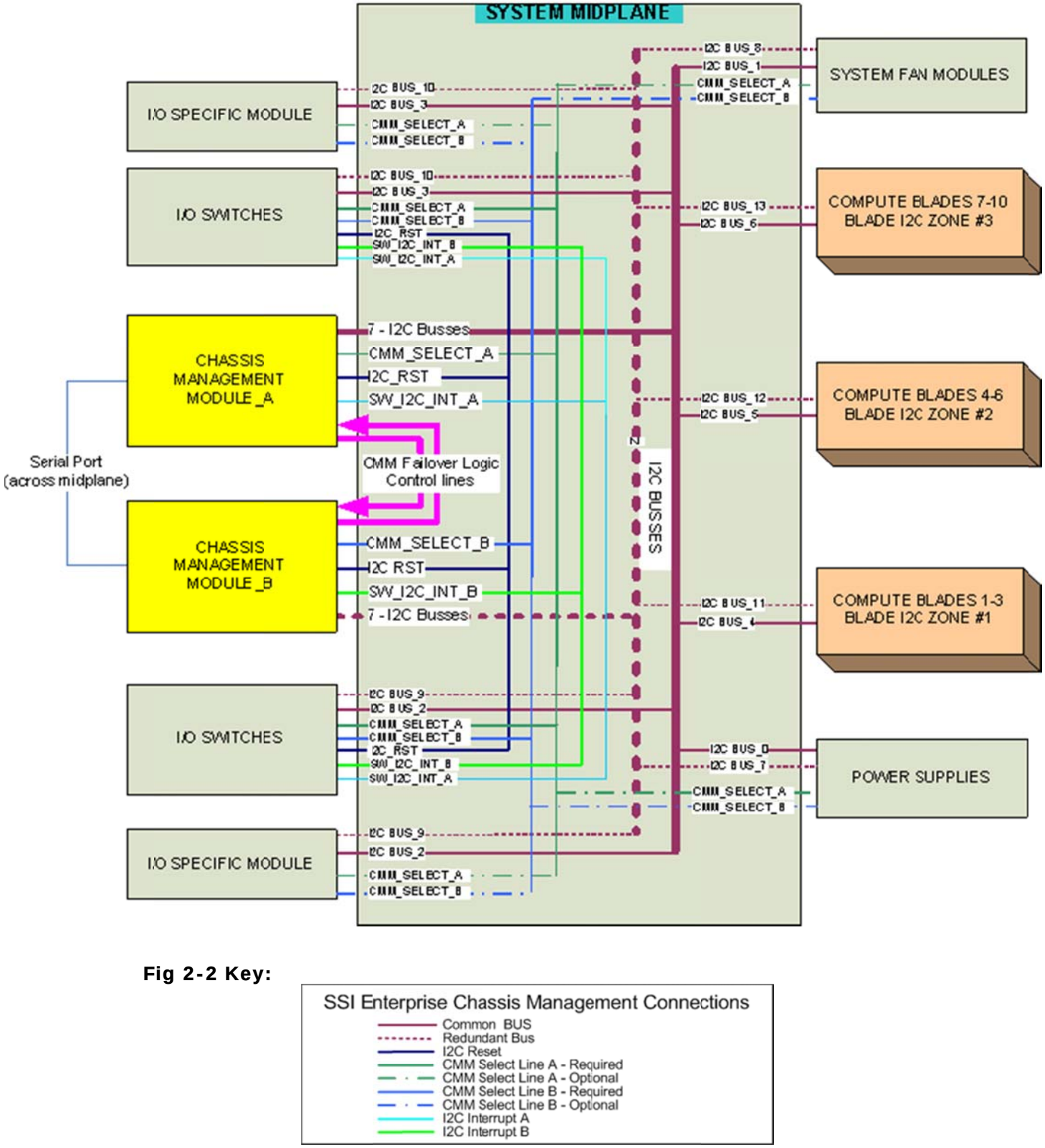


Fig 2-2 Key:

Figure 2-3: Redundant Ethernet Management System Connections

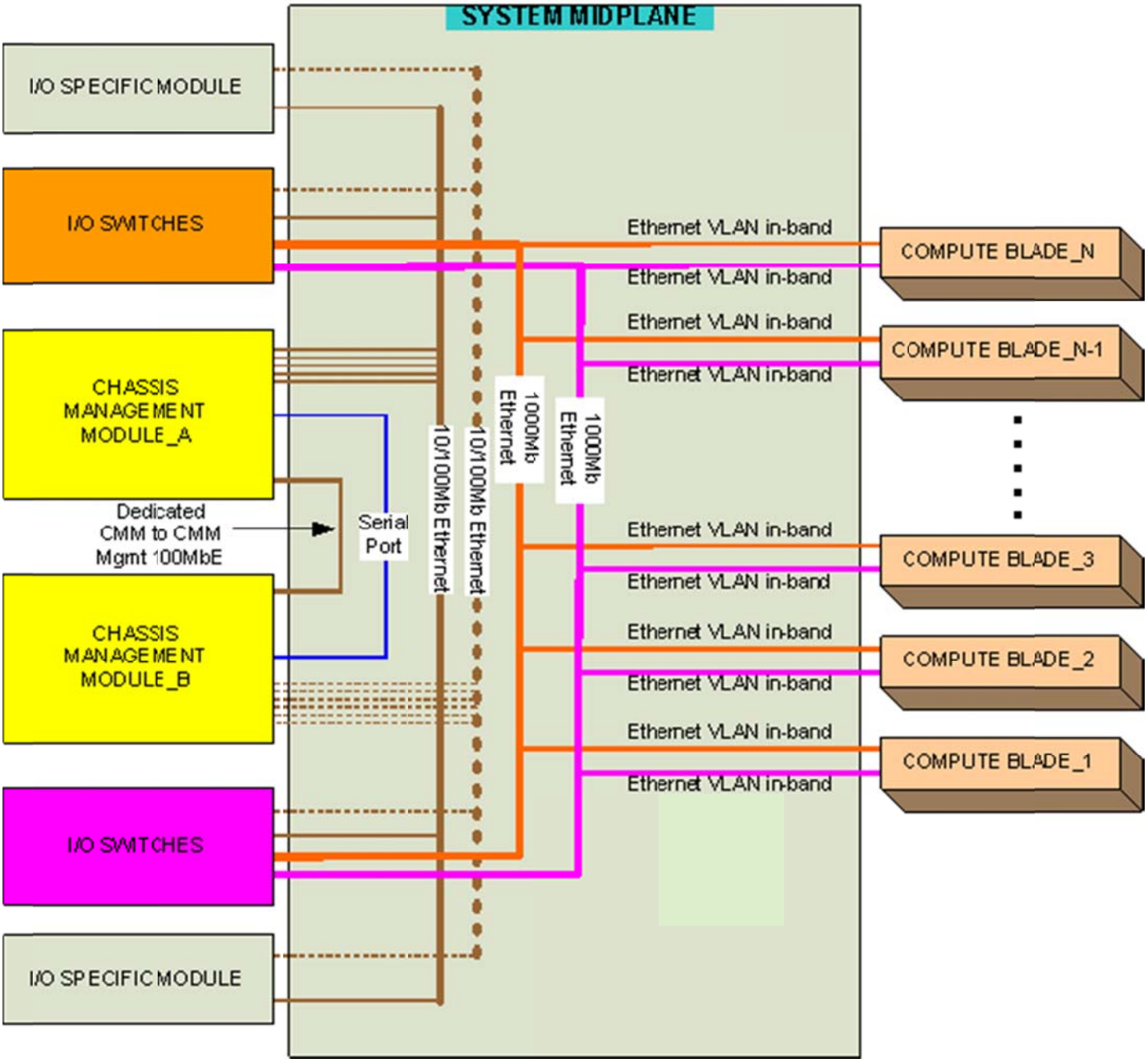


Fig 2-3 Key:

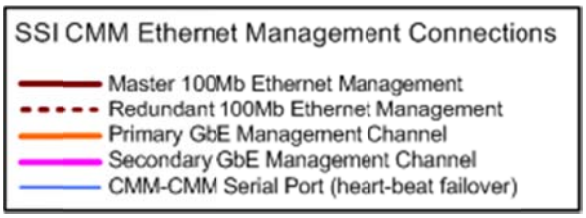


Figure 2-4 shows what the logical connections would look like in a non-redundant system.

Figure 2-4: Non-Redundant CMM Management Connection Diagram

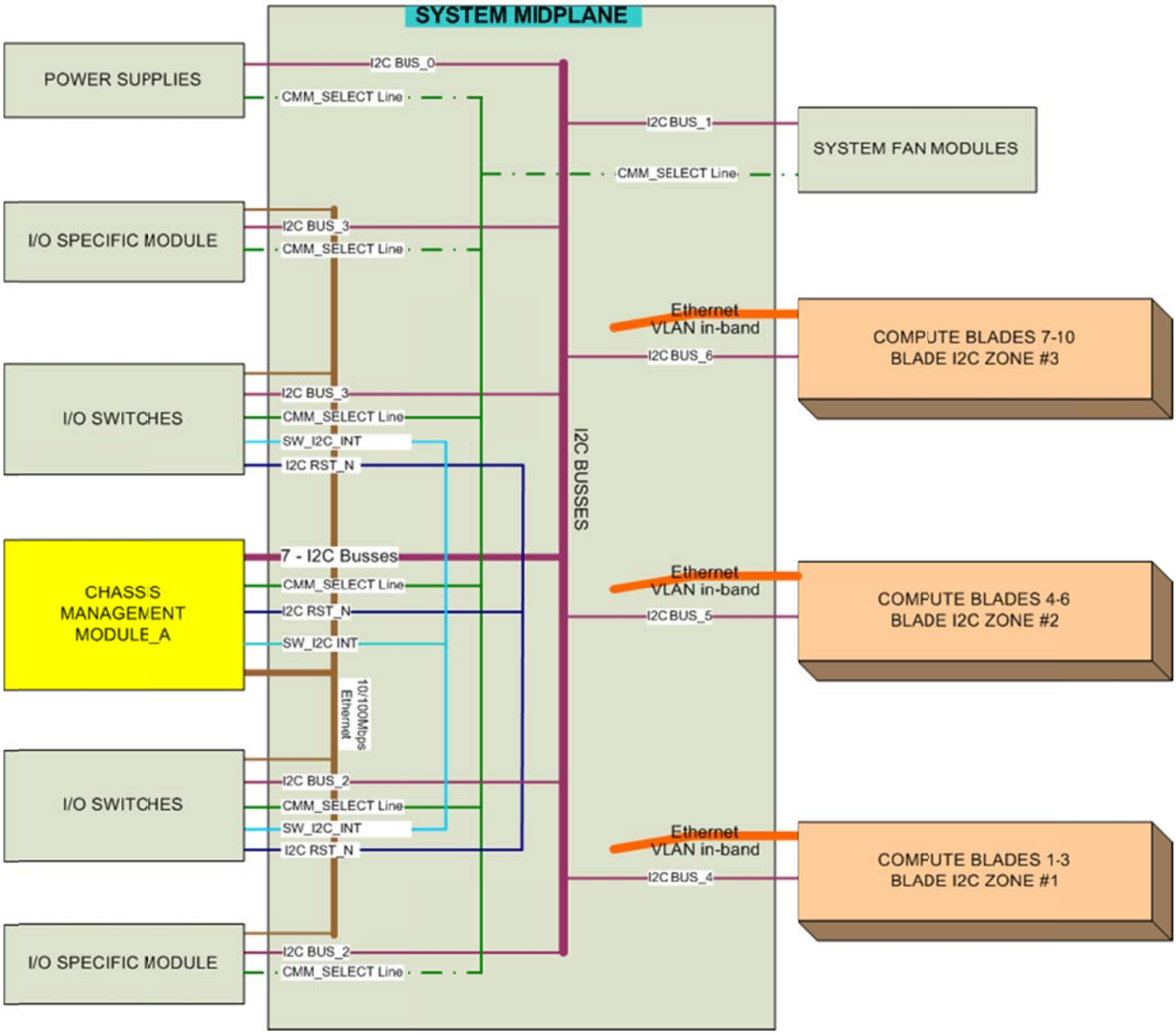


Fig 2-4 Key:

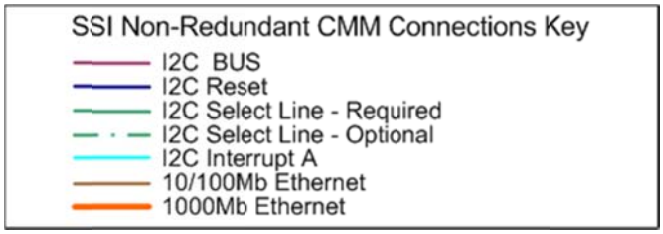
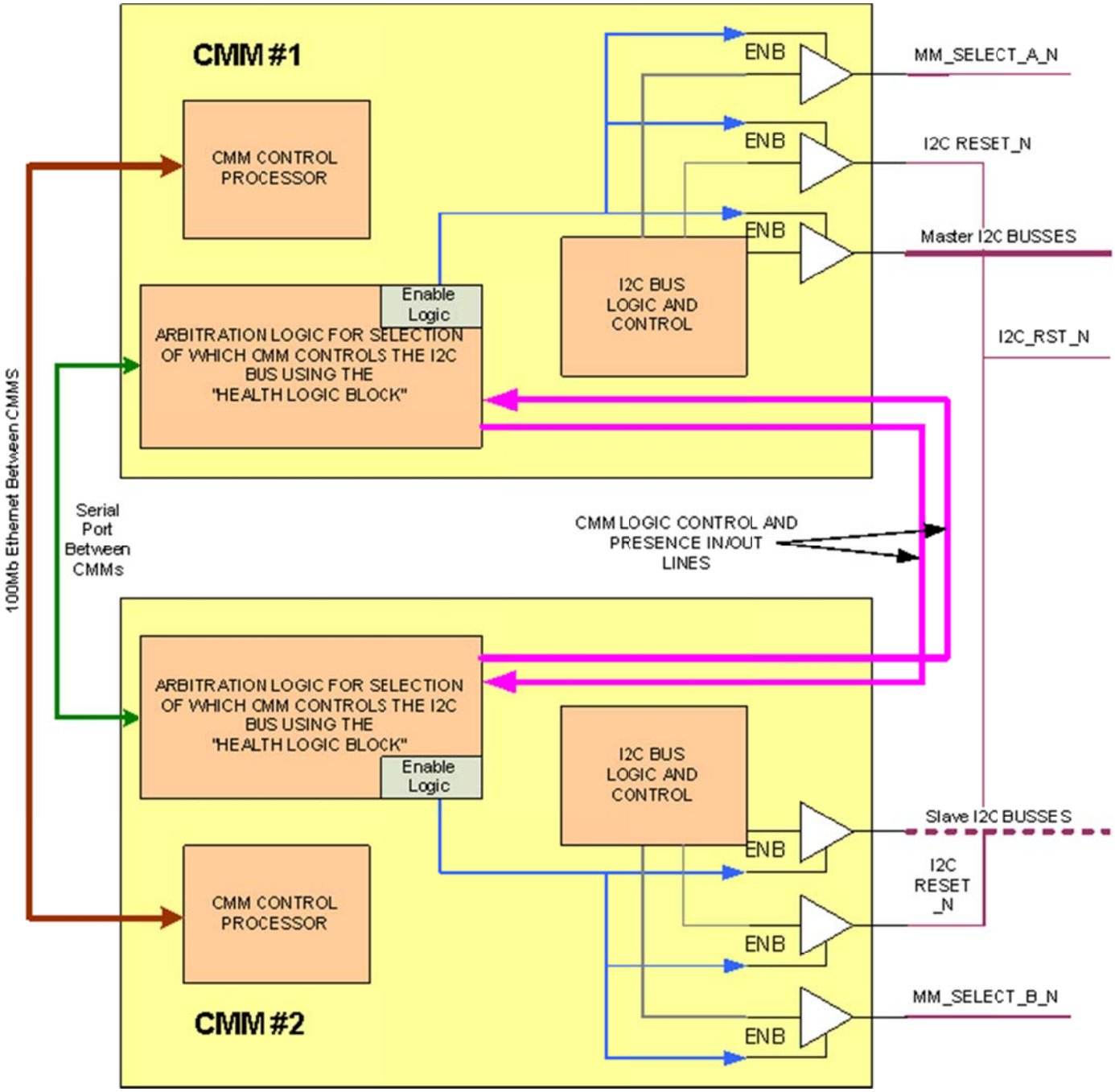


Figure 2-5 shows a diagram of the I2C bus arbitration and control functions. See the detailed description in Section 3.2.

Figure 2-5: I2C Arbitration and Control Diagram



2.1.2 CMM Arbitration Logic Functional Description

An asynchronous serial port connects the two CMMs, along with a dedicated Ethernet channel (100 Mbps). They are used to pass system state information between the CMMs. In addition, two logic lines connect the CMMs, which help the modules determine between themselves their health and state. All of these signals are used by the Arbitration Logic block to determine which of the CMMs is the primary and which is on standby.

The I2C Bus Logic and Control block provides the I2C bus functionality. This could be implemented in a larger CPLD, a smaller FPGA, or it could be a micro-controller that provides the I2C bus outputs.

Each of the I2C bus outputs (SDA and SCL) needs to be controlled by a tri-state type device that will allow the isolation of that bus from the system via the Arbitration and Control logic. When one CMM is determined to be the standby module, its associated I2C bus should NOT be enabled to drive the bus.

2.1.3 CMM Failover Logic

Figure 2-6 (below) shows a block diagram of the logic to be implemented to have a successful fail-over in a system with redundant CMMs.

The operation of the logic control is briefly described.

Presence IN/OUT lines are used to detect the presence of the other CMM, and to give the presence signal to the other CMM.

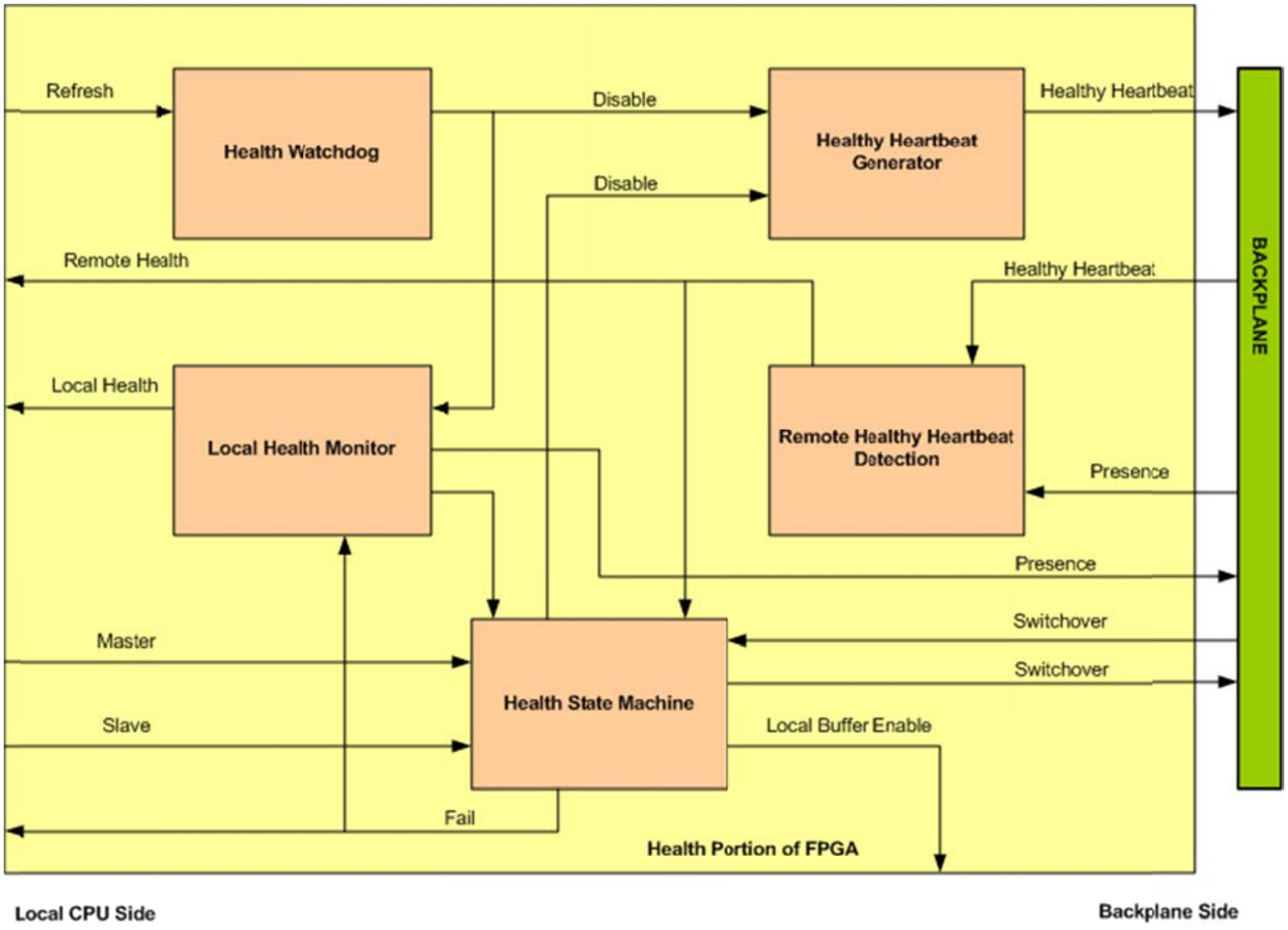
Healthy Heartbeat IN/OUT signals are accomplished via the serial port (RS-232) between the CMMs.

Switchover Logic IN/OUT signals are used to control which of the CMMs is the Master CMM, and which is the Slave.

The failover logic must be capable of switching control of a non-functional CMM from having been Master to a Slave status, regardless of the operational condition of that CMM.

As noted in section 2.1, both CMMs **shall** be of the same manufacturer; i.e. they must be the same hardware and software implementation.

Figure 2-6: Failover Logic Control Diagram



Simplified Health Block Diagram

2.2 CMM Mechanical Specifications

The CMM consists of a mechanical enclosure with a printed board assembly mounted in the enclosure.

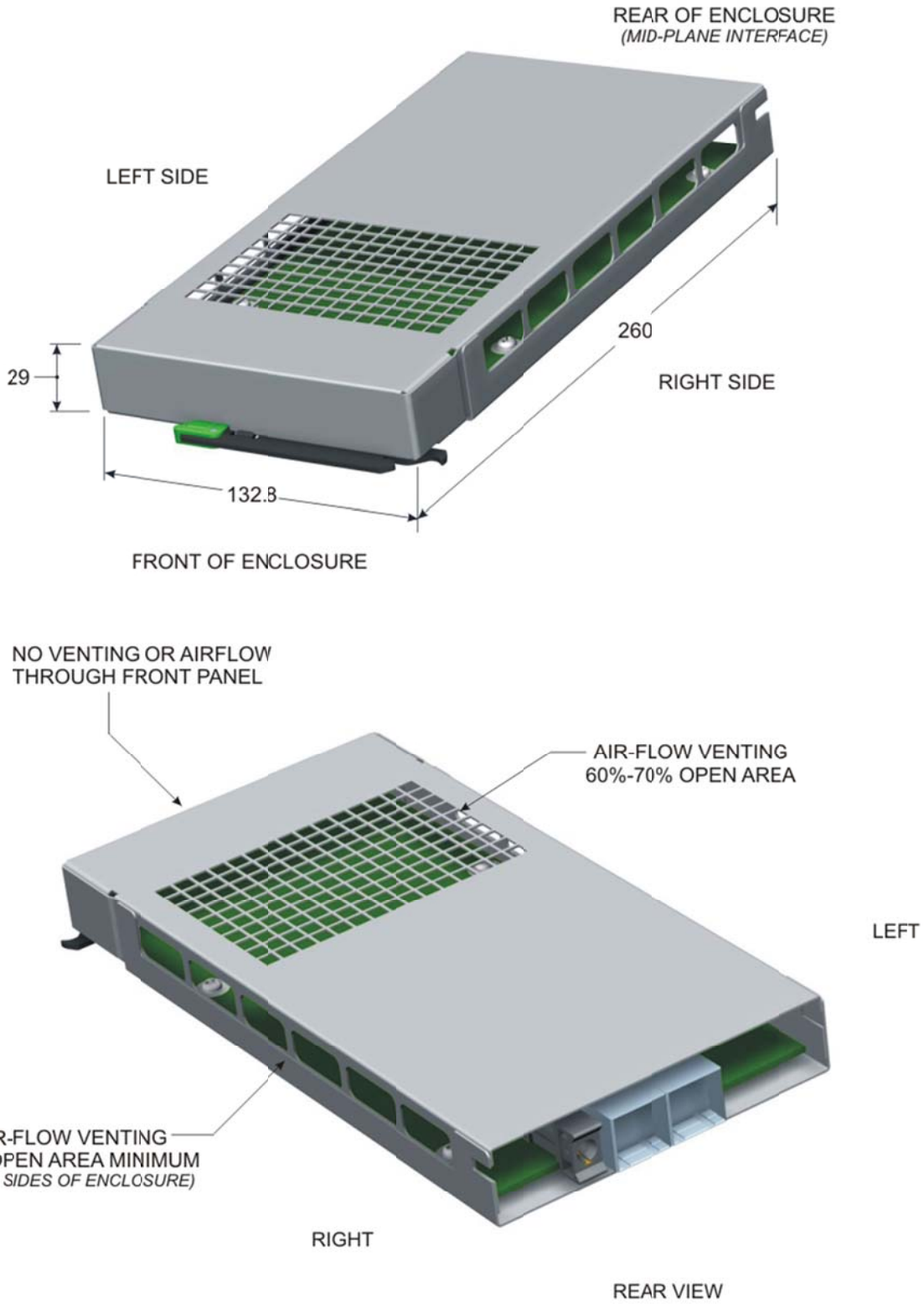
The electro/mechanical interface to the system mid-plane board is accomplished with two Airmax* 120-pin (4-pair) signal connectors, using an Airmax guide pin on the mid-plane. A receiving guide pin module on the CMM PBA guarantees alignment.

Maximum power for the module is defined at 50 W TDP.

2.2.1 CMM Enclosure Mechanical Details

Figure 2-7 illustrates the CMM enclosure.

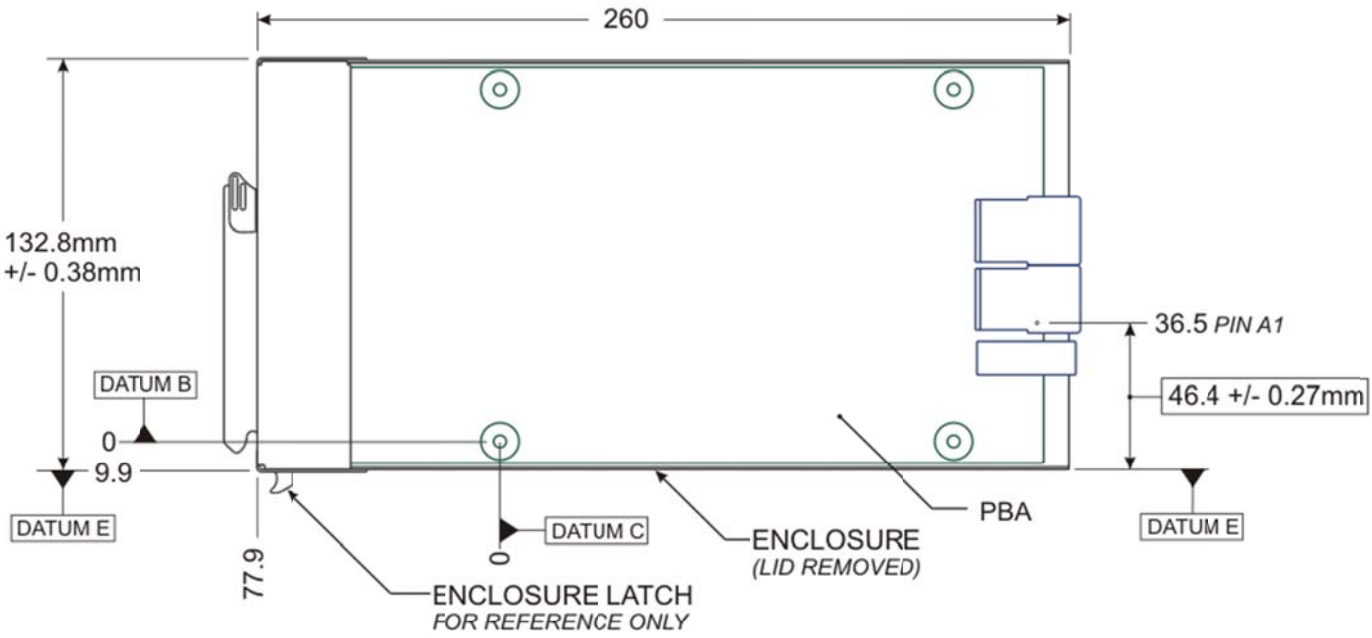
Figure 2-7: Enclosure Isometric Views



Figures 2-8 through 2-14 define the size constraints for the CMM PCB. Also defined is a maximum component height area for the secondary side of the PBA. This location is required for the secondary side of the PBA only. Dimensional clearances to prevent component and enclosure interferences are provided in Figure 2-9.

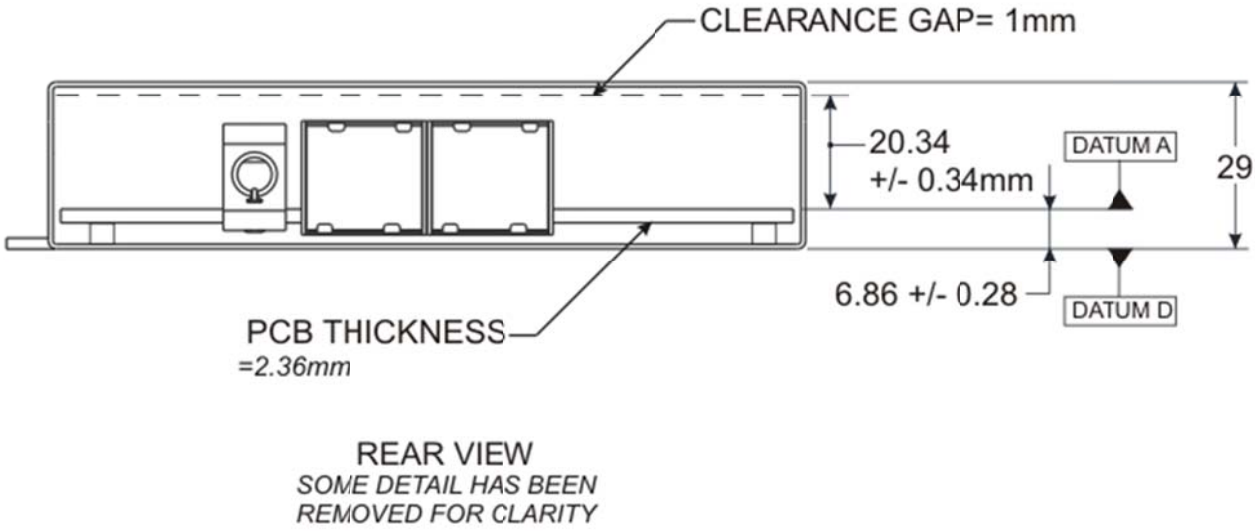
Datum 'B' and Datum 'C' (Figure 2-8) locate the primary mounting hole from which the I/O connectors are referenced. Furthermore, the PBA-to-enclosure interface is referenced using these two datums. Datum 'E' references the enclosure's primary side mounting surface, and provides the required dimension between Datum 'E' and pin A1 of the main signal connector. This required dimension minimizes tolerance stack in an attempt to ensure a reliable and repeatable interface between the CMM, the server system mid-plane PBA, and the blade server system chassis. See Figures 2-8 through 2-14 for reference.

Figure 2-8: Enclosure Mechanical sketch



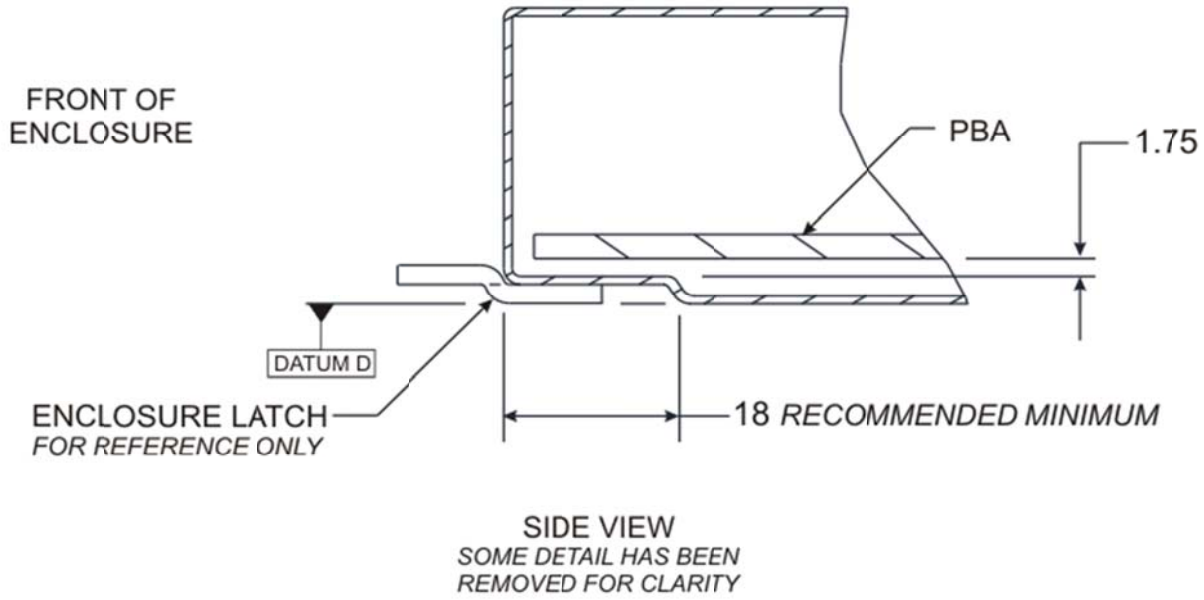
See Figure 2-9 below. Datum 'A' is defined as the primary component side of the CMM PWB. The relationship between Datum 'A' and the bottom side mounting surface of the CMM is defined using Datum 'D' as shown in Figure 2-9. This required dimension minimizes tolerance stack in an attempt to ensure a reliable and repeatable interface between the CMM and the blade server system when the CMM is installed in this orientation.

Figure 2-9: Enclosure Mechanical Rear (Mid-plane) View



A localized offset area **shall** be included in the front portion of the CMM enclosure, as shown in Figure 2-10. The offset allows room for the enclosure latch to fit within the overall CMM module envelope. Special care must be taken to ensure that the PBA components, such as through-hole component leads, **shall not** protrude through the PWB and contact the sheet metal in this area.

Figure 2-10: Enclosure Mechanical Side View Details



2.2.2 Mechanical Enclosure Latch details

Figure 2-11 illustrates the latch mechanical detail.

Figure 2-11: Enclosure Latch - Isometric

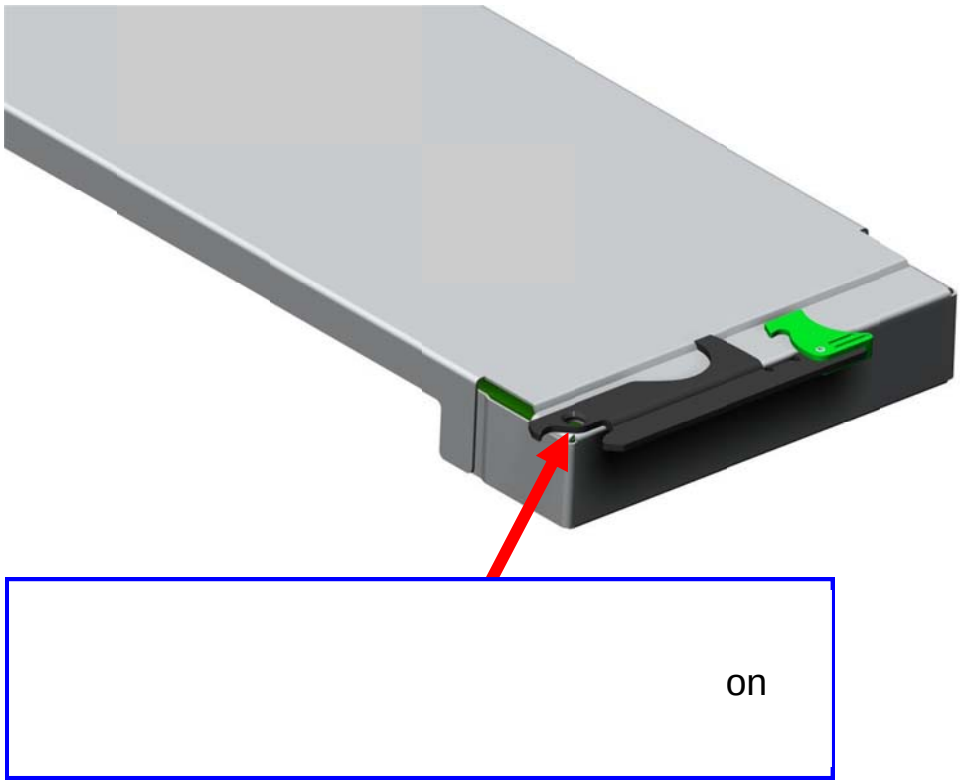
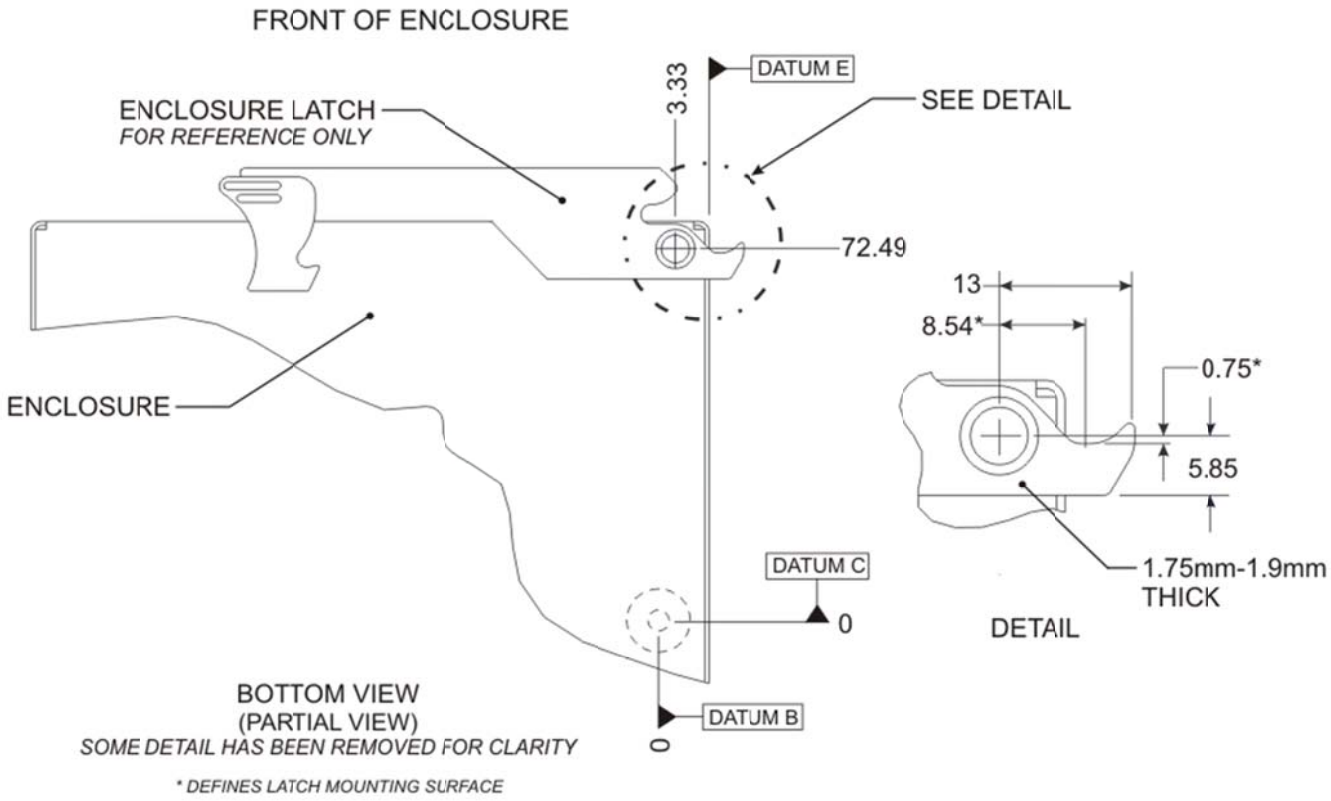


Figure 2-12 describes the engagement portion of a typical latch relative to the enclosure and to Datum 'B' and Datum 'C'. To ensure reliable latching between the CMM enclosure and the blade server system, the latch mounting details should be copied as closely as possible. Although use of this reference design is not required for specification compliance, it is highly recommended to ensure reliable and robust performance during insertion and extraction of the CMM module.

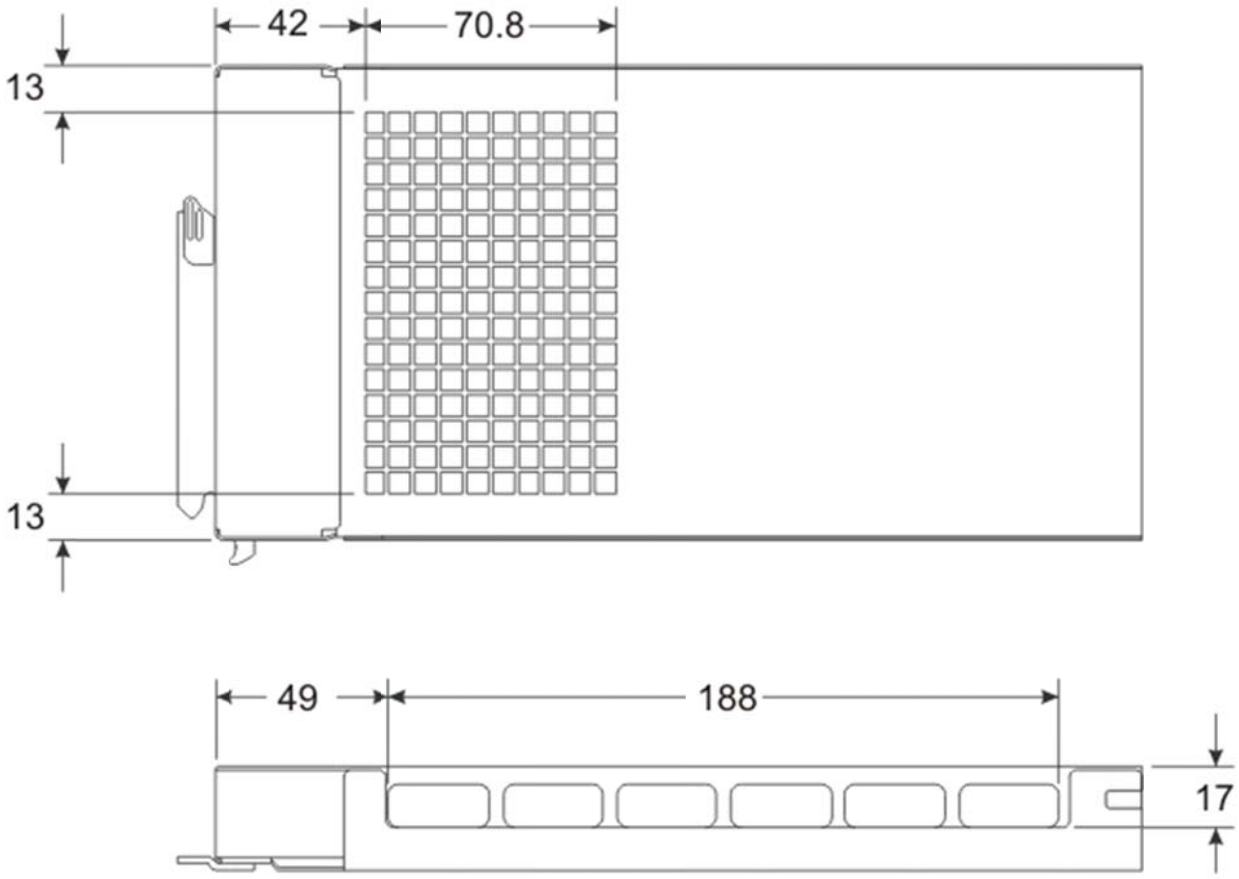
Figure 2-12: Enclosure Latch Details



2.2.3 Mechanical Enclosure Venting Requirements

Figure 2-13 describes the venting required to allow sufficient airflow through the CMM. All defined venting is required such that all SSI-compliant air flow paths are supported. Chassis solutions, at the discretion of system developers, may or may not leverage all required CMM enclosure venting to achieve proper cooling.

Figure 2-13: Enclosure Mechanical Venting



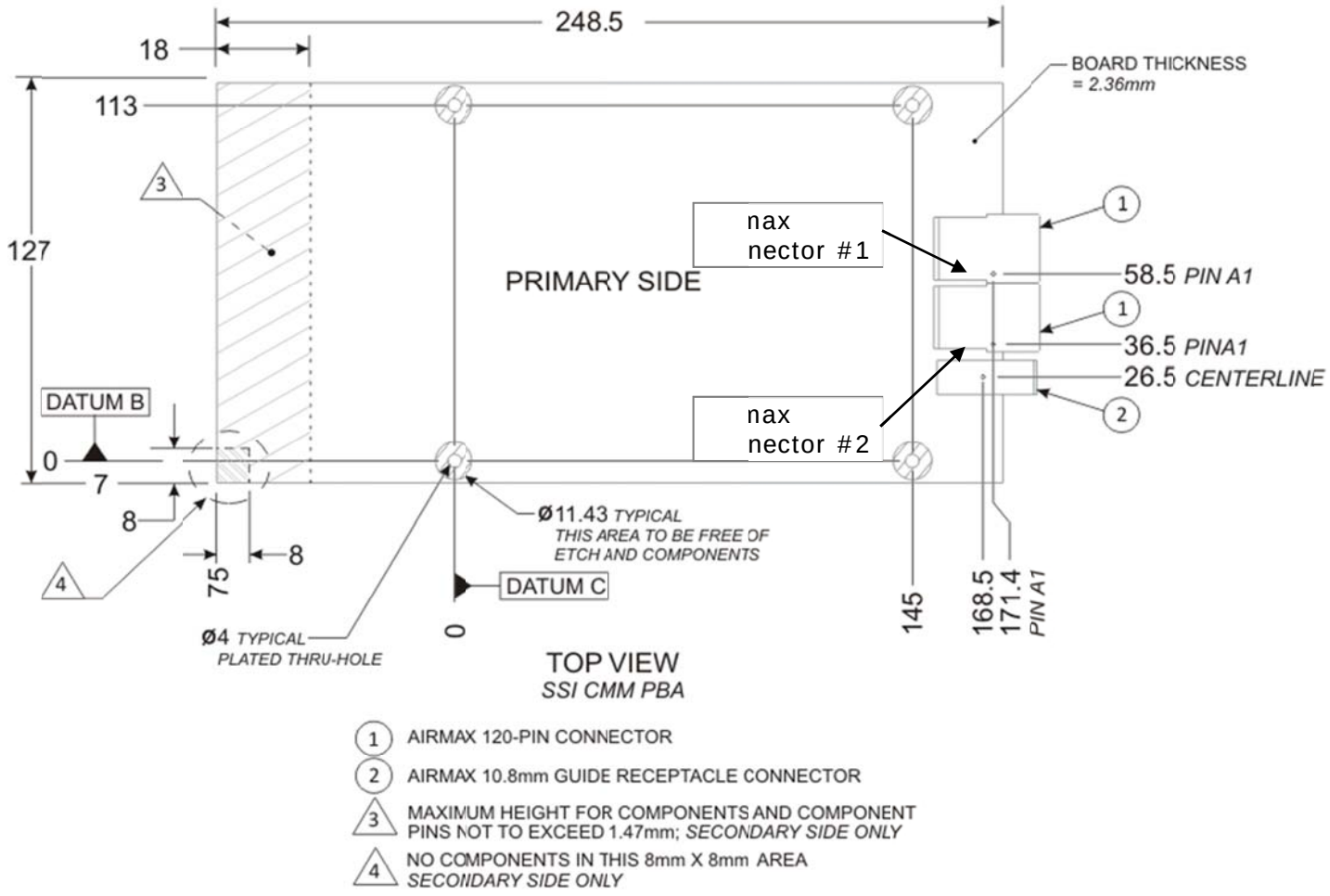
2.2.4 Printed Circuit Board Assembly (PBA) Requirements

The PBA required mechanical definition is shown below.

Figure 2-14 defines the size constraints for the CMM PCB. Also defined is a maximum component height area for the secondary side of the PBA. This location is required for the secondary side of the PBA only. Dimensional clearances to prevent component and enclosure interferences are provided in Figure 2-9.

Airmax connector labeled “1” in Figure 2-14 corresponds to Connector #1 in Section 2.3.2, Figure 2-17. Airmax connector labeled “2” in Figure 2-14 corresponds to Connector #2 in Section 2.3.2, Figure 2-18.

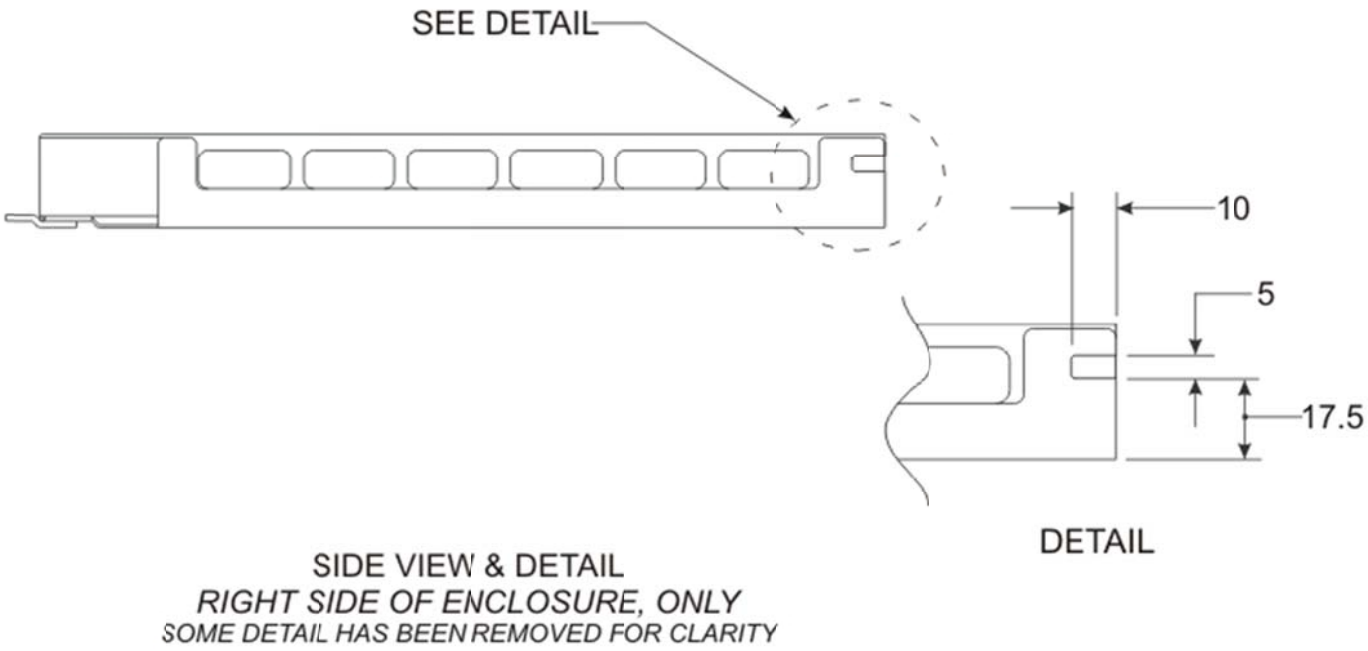
Figure 2-14: PBA Mechanical Sketch



2.2.5 Mechanical Enclosure Keying

The CMM enclosure **shall** be keyed in order to prevent incorrect insertion of the CMM into the blade server system. See Figure 2-15 for details.

Figure 2-15: Mechanical Enclosure Keying Details



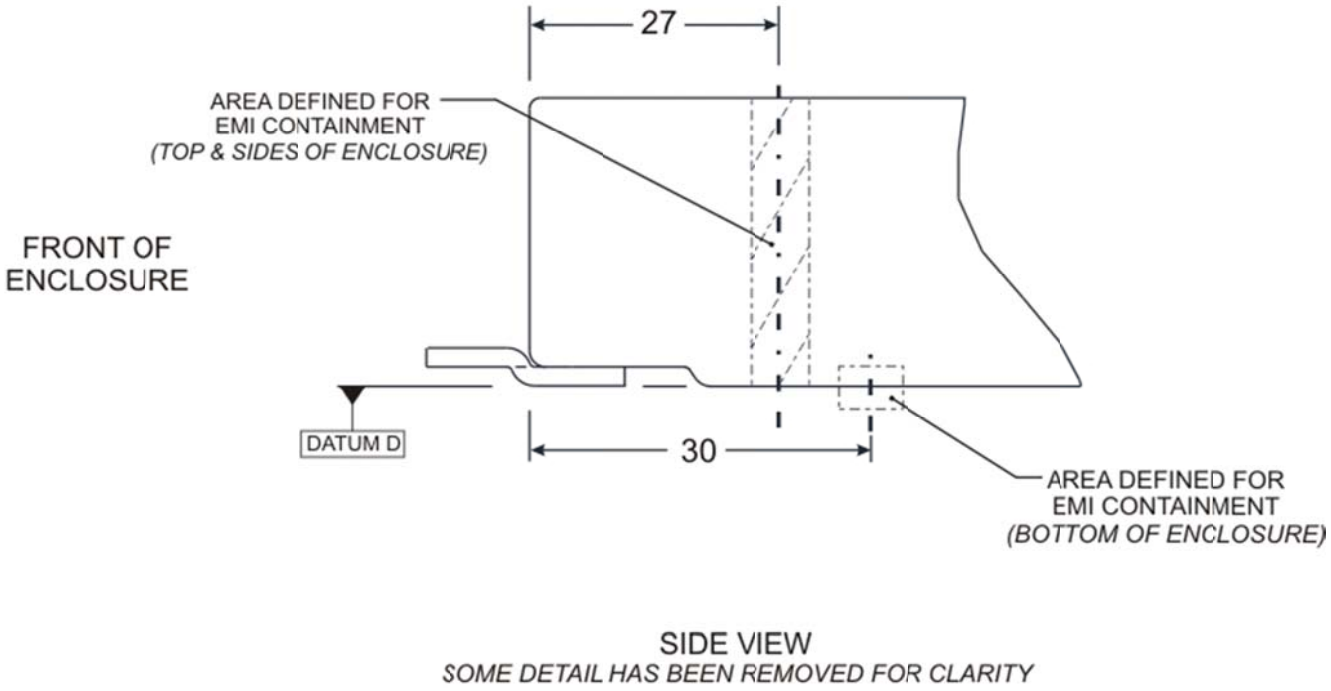
SIDE VIEW & DETAIL
RIGHT SIDE OF ENCLOSURE, ONLY
SOME DETAIL HAS BEEN REMOVED FOR CLARITY

2.2.6 Mechanical EMI Gasket Requirement

The CMM enclosure should have provision for the addition of an EMI gasket within the system to pass electromagnetic emissions testing requirements.

See Figure 2-16 for gasket location details.

Figure 2-16: Enclosure EMI Gasket Details



SIDE VIEW
SOME DETAIL HAS BEEN REMOVED FOR CLARITY

For the gasket material/solution, the height of such material **shall** be 3.5 mm.

2.3 CMM Electrical Connector Definition

2.3.1 Connector Types

The CMM uses two 120-pin, 4-pair, Airmax connectors for signal and power connections to the system mid-plane, with a single guide pin and receiving module to guarantee connector alignment with the mid-plane. Table 2-1 lists the connector types, manufacturers, and part numbers for different CMM connectors.

Table 2-1: Connector Reference Table

Connector	Description	Manufacturer	Part Number
Mid-plane Signal Interface	Airmax, right-angle, 2 mm, 4-pair, 120-pin with short pin detect.	FCI*	10084600-111LF
Guide Pin Receptacle	10.8 mm guide pin receptacle without ESD clip	FCI*	10084609-111LF
Serial Port D-Sub	Industry-standard 9-pin, D-sub serial port connector, female Note: Use straight-through cable with cross-over done in hardware layout.	Many	Many
Ethernet connector	RJ-45 Ethernet connector	Many	Many

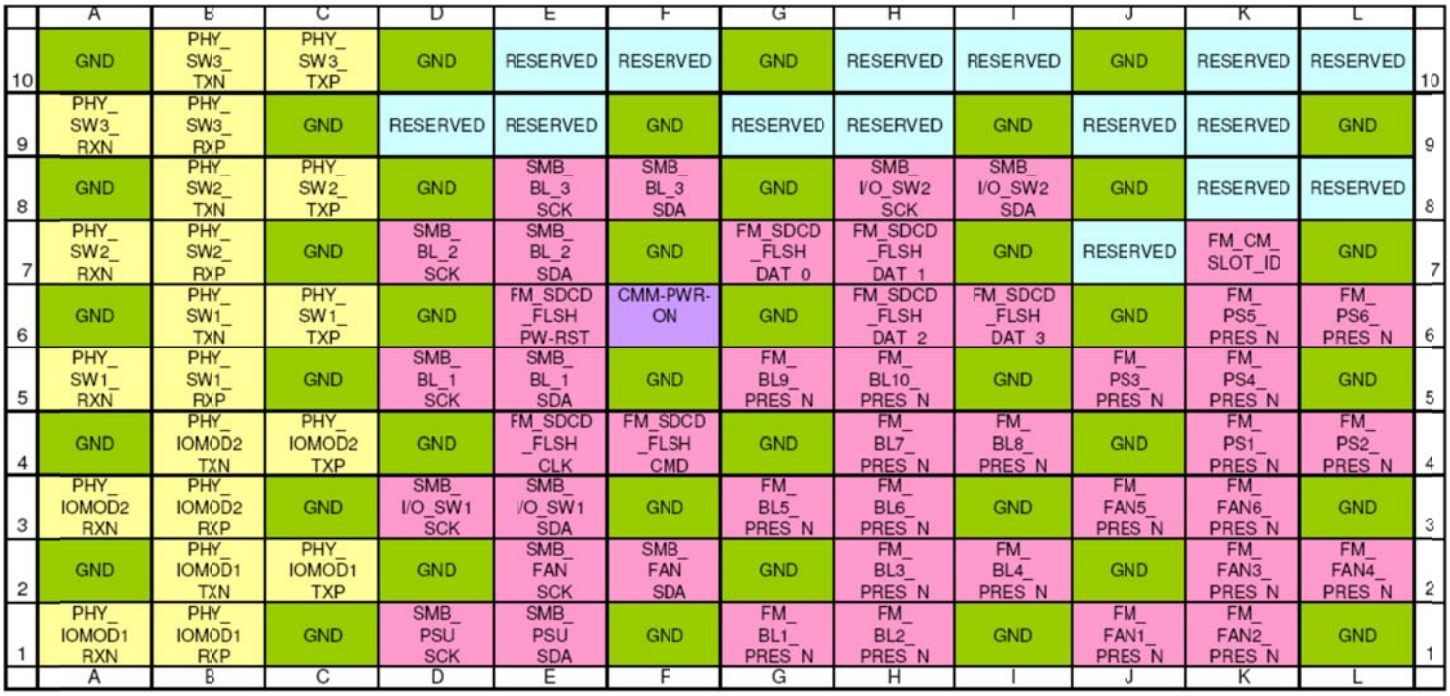
2.3.2 Signal Connector Pinout Definition

Figure 2-17 defines the mid-plane connector #1 pinout. Figure 2-18 defines the mid-plane connector #2 pinout. Table 2-2 defines the CMM connector signals for connectors #1 and #2. Table 2-3 defines the mid-plane connector signals. See Figure 2-14 in Section 2.2 for identification of connector placement and location within the module.

Figure 2-17: Mid-plane Connector #1 Pinout Definition

	A	B	C	D	E	F	G	H	I	J	K	L	
10	GND	RESERVED	RESERVED	GND	P12V	P12V	GND	P12V	P12V	GND	P12V	P12V	10
9	RESERVED	RESERVED	GND	CMM_ HLTH_HB_ OUT	CMM_ HLTH_HB_ IN	GND	P12V	P12V	GND	P12V	P12V	GND	9
8	GND	PHY_ CMM_ TXN	PHY_ CMM_ TXP	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	8
7	PHY_ CMM_ RXN	PHY_ CMM_ RXP	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	7
6	GND	PHY_ SW6_ TXN	PHY_ SW6_ TXP	GND	FM_SW _I2C_ INT_A/B	FM_I2C_ RESET_N	GND	FM_CMM_ CHASSIS_ ID_LED_N	FM_CMM_ CHASSIS_ FLT_LED_N	GND	FM_CMM SELECT A/B_N	RESERVED	6
5	PHY_ SW6_ RXN	PHY_ SW6_ RXP	GND	FM_ IO_1 PRES_N	FM_ IO_2 PRES_N	GND	FM_CMM_ CHASSIS_ PWR-ON	FM_CMM_ FRTPNL_ PRES_N	GND	FM_ BL_9 SPARE	FM_ BL_10 SPARE	GND	5
4	GND	PHY_ SW5_ TXN	PHY_ SW5_ TXP	GND	FM_CM_ PRES_ N_OUT	FM_CM_ PRES_ N_IN	GND	SMB_CMM _LOGIC_ CTL_IN	SMB_CMM _LOGIC_ CTL_OUT	GND	FM_ BL_7 SPARE	FM_ BL_8 SPARE	4
3	PHY_ SW5_ RXN	PHY_ SW5_ RXP	GND	FM_ SW5 PRES_N	FM_ SW6 PRES_N	GND	SMB_ SPARE SCK	SMB_ SPARE SDA	GND	FM_ BL_5 SPARE	FM_ BL_6 SPARE	GND	3
2	GND	PHY_ SW4_ TXN	PHY_ SW4_ TXP	GND	FM_ SW3 PRES_N	FM_ SW4 PRES_N	GND	SER_ PORT_ RTS	SER_ PORT_ CTS	GND	FM_ BL_3 SPARE	FM_ BL_4 SPARE	2
1	PHY_ SW4_ RXN	PHY_ SW4_RXP	GND	FM_ SW1 PRES_N	FM_ SW2 PRES_N	GND	SER_ PORT_ TX	SER_ PORT_ RX	GND	FM_ BL_1 SPARE	FM_ BL_2 SPARE	GND	1
	A	B	C	D	E	F	G	H	I	J	K	L	

Figure 2-18: Mid-plane Connector #2 Pinout Definition



	A	B	C	D	E	F	G	H	I	J	K	L	
10	GND	PHY_SW3_TXN	PHY_SW3_TXP	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	10
9	PHY_SW3_RXN	PHY_SW3_RXP	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	RESERVED	RESERVED	GND	9
8	GND	PHY_SW2_TXN	PHY_SW2_TXP	GND	SMB_BL_3 SCK	SMB_BL_3 SDA	GND	SMB_I/O_SW2 SCK	SMB_I/O_SW2 SDA	GND	RESERVED	RESERVED	8
7	PHY_SW2_RXN	PHY_SW2_RXP	GND	SMB_BL_2 SCK	SMB_BL_2 SDA	GND	FM_SDCD_FLSH DAT_0	FM_SDCD_FLSH DAT_1	GND	RESERVED	FM_CM_SLOT_ID	GND	7
6	GND	PHY_SW1_TXN	PHY_SW1_TXP	GND	FM_SDCD_FLSH PW-RST	CMM-PWR-ON	GND	FM_SDCD_FLSH DAT_2	FM_SDCD_FLSH DAT_3	GND	FM_PS5_PRES_N	FM_PS6_PRES_N	6
5	PHY_SW1_RXN	PHY_SW1_RXP	GND	SMB_BL_1 SCK	SMB_BL_1 SDA	GND	FM_BL9_PRES_N	FM_BL10_PRES_N	GND	FM_PS3_PRES_N	FM_PS4_PRES_N	GND	5
4	GND	PHY_IOMOD2 TXN	PHY_IOMOD2 TXP	GND	FM_SDCD_FLSH CLK	FM_SDCD_FLSH CMD	GND	FM_BL7_PRES_N	FM_BL8_PRES_N	GND	FM_PS1_PRES_N	FM_PS2_PRES_N	4
3	PHY_IOMOD2 RXN	PHY_IOMOD2 RXP	GND	SMB_I/O_SW1 SCK	SMB_I/O_SW1 SDA	GND	FM_BL5_PRES_N	FM_BL6_PRES_N	GND	FM_FAN5_PRES_N	FM_FAN6_PRES_N	GND	3
2	GND	PHY_IOMOD1 TXN	PHY_IOMOD1 TXP	GND	SMB_FAN SCK	SMB_FAN SDA	GND	FM_BL3_PRES_N	FM_BL4_PRES_N	GND	FM_FAN3_PRES_N	FM_FAN4_PRES_N	2
1	PHY_IOMOD1 RXN	PHY_IOMOD1 RXP	GND	SMB_PSU SCK	SMB_PSU SDA	GND	FM_BL1_PRES_N	FM_BL2_PRES_N	GND	FM_FAN1_PRES_N	FM_FAN2_PRES_N	GND	1
	A	B	C	D	E	F	G	H	I	J	K	L	

Table 2-2: CMM Connector Signal Descriptions

Pin Number	Signal Name	Signal Type & Polarity	Description / Definition
Connector #1 Pins A1/B1	PHY_SW4_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #4
Connector #1 Pins B2/C2	PHY_SW4_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #4
Connector #1 Pins A3/B3	PHY_SW5_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #5
Connector #1 Pins B4/C4	PHY_SW5_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #5
Connector #1 Pins A5/B5	PHY_SW6_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #6
Connector #1 Pins B6/C6	PHY_SW6_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #6
Connector #1 Pins A7/B7	PHY_CMM_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to CMM. These lines will have to be routed between the CMMs to route RXP/N to TXP/N
Connector #1 Pins B8/C8	PHY_CMM_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to CMM. These lines will have to be routed between the CMMs to route TXP/N to RXP/N
Connector #1 Pins:G9,H9,J9,K9, E10,F10,H10,I10, K10,L10	P12V	Power, +12 V	+12V DC power from mid-plane
Connector #1 Pin D1	FM_SW1_PRES_N	Static 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW1 Module position, pulled down when switch is inserted into slot. LVTTL level signal.
Connector #1 Pin E1	FM_SW2_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW2 Module position, pulled down when switch is

Pin Number	Signal Name	Signal Type & Polarity	Description / Definition
			inserted into slot. LVTTL level signal.
Connector #1 Pin E2	FM_SW3_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW3 Module position, pulled down when switch is inserted into slot. LVTTL level signal.
Connector #1 Pin F2	FM_SW4_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW4 Module position, pulled down when switch is inserted into slot. LVTTL level signal.
Connector #1 Pin D3	FM_SW5_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW5 Module position, pulled down when switch is inserted into slot. LVTTL level signal.
Connector #1 Pin E3	FM_SW6_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect into the CMM from the SW6 Module position, pulled down when switch is inserted into slot. LVTTL level signal.
Connector #1 Pin E4	FM_CM_PRES_N_ OUT	OUTPUT, 3.3 V Pullup on mid-plane.	CMM Present Detection signal to the OTHER CMM. This CMM PULLS this signal down when inserted into the chassis. LVTTL level signal.
Connector #1 Pin F4	FM_CM_PRES_N_ IN	INPUT, 3.3 V Pullup on mid-plane. Should be open collector input.	CMM Present Detection signal to THIS CMM indicating that the other CMM is present, pulled down when OTHER CMM is inserted into Chassis slot. LVTTL level signal.
Connector #1 Pin D5	FM_IO_1_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect signal for IO Slot #1. LVTTL level signal. (If I/O Slots are included in design)
Connector #1 Pin E5	FM_IO_2_PRES_N	INPUT, 3.3 V Pullup on mid-plane.	Present detect signal for IO Slot #2. LVTTL level signal. (If I/O Slots are included in design)
Connector #1 Pin E6	FM_SW_I2C_INT_ A/B	INPUT, 5V Pullup on mid-plane. Open collector Input. Active LOW.	I2C Interrupt line from any of the SSI-compatible switches to either the CMM A, or CMM B I2C controller. 5V Logic level signal.
Connector #1 Pin F6	FM_I2C_RESET_N	OUTPUT, 5 V Pullup on mid-plane. Open collector Output.	Shared line from either CMM that forces all of the switch modules to clear their I2C controllers. 5V Logic level signal.
Connector #1 Pins D9/E9	CMM_HLTH_HB_ OUT/IN	A health Status line between the CMMs. The “OUT” line goes to the other CMM, the “IN” line is from the other CMM. 3.3 V Logic level.	Logic control lines that report the health heart-beat of the existing CMM to the other CMM and receive the health heartbeat status from the other CMM for part of the determination of the master CMM. LVTTL level.
Connector #1 Pin G1	SER_PORT_TX	OUTPUT, Serial port data output.	CMM to CMM Serial Port – TX output.
Connector #1 Pin H1	SER_PORT_RX	INPUT, Serial port data input.	CMM to CMM Serial Port – RX input.
Connector #1 Pin H2	SER_PORT_RTS	INPUT, Serial port control input.	CMM to CMM Serial Port – RTS signal.
Connector #1 Pin I2	SER_PORT_CTS	OUTPUT, Serial port control output.	CMM to CMM Serial Port – CTS signal.
Connector #1 Pin G3	SMB_SPARE_SCK	OUTPUT, 5V Pullup on mid-plane. Open Collector output.	Spare I2C Clock Pin for system design currently unused. **Shall** be 5V TTL level signal if used.
Connector #1 Pin H3	SMB_SPARE_SDA	IN/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	Spare I2C Data Pin for system design currently unused. 5V TTL level signal.
Connector #1 Pin H4	SMB_CMM_CTL_ IN	INPUT, 3.3 V Pullup on mid-plane. Open Collector input. LVTTL level signal	CMM to CMM Logic control signal for I2C Arbitration logic to determine which CMM controls the I2C bus communications. This signal is an input FROM the OTHER CMM.
Connector #1	SMB_CMM_CTL_	OUTPUT, 3.3 V Pullup on	CMM to CMM Logic control signal for I2C

<table>
<tr><th>Pin Number</th><th>Signal Name</th><th>Signal Type & Polarity</th><th>Description / Definition</th></tr>
<tr><td>Pin I4</td><td>OUT</td><td>mid-plane.
Open Collector output.
LVTTL level signal</td><td>Arbitration logic to determine which CMM controls the I2C bus communications. This signal is an output TO the OTHER CMM.</td></tr>
<tr><td>Connector #1
Pin G5</td><td>FM_CMM_CHASSIS_PWR-ON</td><td>INPUT, 3.3 V Logic signal from Front Panel controller (if used). LVTTL level signal</td><td>Chassis power on input line from the chassis front panel.</td></tr>
<tr><td>Connector #1
Pin H5</td><td>FM_CMM_FRTPNL_PRES_N</td><td>INPUT, 3.3 V Pullup on mid-plane.</td><td>Present detect into the CMM from the Front Panel board (if used). Pulled down when Front Panel board is present in the system.
LVTTL level signal.</td></tr>
<tr><td>Connector #1
Pin H6</td><td>FM_CMM_CHASSIS_ID_LED_N</td><td>OUTPUT, LED drive signal to LED with 3.3 V Pullup.</td><td>Chassis ID LED output line for the Chassis ID LED (used to light the Chassis ID LED).
Shall sink a minimum current of 15mA.</td></tr>
<tr><td>Connector #1
Pin I6</td><td>FM_CMM_CHASSIS_FLT_LED_N</td><td>OUTPUT, LED drive signal to LED with 3.3 V Pullup.</td><td>Chassis Fault line output line for the Chassis Fault LED (used to light the Chassis Fault LED)
Shall sink a minimum current of 15mA.</td></tr>
<tr><td>Connector #1
Pin J1</td><td>FM_BL_1_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #1</td><td>Blade #1 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin K1</td><td>FM_BL_2_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #2</td><td>Blade #2 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin K2</td><td>FM_BL_3_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #3</td><td>Blade #3 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin L2</td><td>FM_BL_4_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #4</td><td>Blade #4 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin J3</td><td>FM_BL_5_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #5</td><td>Blade #5 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin K3</td><td>FM_BL_6_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #6</td><td>Blade #6 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin K4</td><td>FM_BL_7_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #7</td><td>Blade #7 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin L4</td><td>FM_BL_8_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #8</td><td>Blade #8 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin J5</td><td>FM_BL_9_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #9</td><td>Blade #9 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin K5</td><td>FM_BL_10_SPARE</td><td>Undefined wire reserved for use between CMM and Compute Blade #10</td><td>Blade #10 to CMM Spare Wire pin – this pin should be routed from the blade to the CMM.</td></tr>
<tr><td>Connector #1
Pin: K6</td><td>FM_CMM_SELECT_A/B_N</td><td>5V Logic lines to determine which CMM is the ACTIVE CMM</td><td>
<table>
<tr><th>MM_select_A</th><th>MM_select_B</th><th>ACTIVE I2C I/F</th></tr>
<tr><td>0</td><td>0</td><td>No BUS Active</td></tr>
<tr><td>0</td><td>1</td><td>Bus A Active</td></tr>
<tr><td>1</td><td>0</td><td>Bus B Active</td></tr>
<tr><td>1</td><td>1</td><td>No BUS Active</td></tr>
</table>
</td></tr>
<tr><td>Connector #1
Pins: L6,D7,E7,
G7,H7,J7,K7,E8,</td><td>RESERVED</td><td>Reserved, undefined signal pin.</td><td>Signal pin reserved for future design needs.</td></tr>
</table>

Pin Number	Signal Name	Signal Type & Polarity	Description / Definition
F8,H8,I8,K8,L8, A9,B9,B10,C10			
Connector #2 Pins A1/B1	PHY_IOMOD1_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to IO Module #1
Connector #2 Pins B2/C2	PHY_IOMOD1_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to user-defined I/O Module #1
Connector #2 Pins A3/B3	PHY_IOMOD2_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to user-defined I/O Module #2
Connector #2 Pins B4/C4	PHY_IOMOD2_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to user-defined I/O Module #2
Connector #2 Pins A5/B5	PHY_SW1_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #1
Connector #2 Pins B6/C6	PHY_SW1_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #1
Connector #2 Pins A7/B7	PHY_SW2_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #2
Connector #2 Pins B8/C8	PHY_SW2_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #2
Connector #2 Pins A9/B9	PHY_SW3_ RXN/RXP	INPUT, SERDES, 100 ohm differential	SERDES Receive Ethernet diff-pair signal from CMM to Ethernet Switch #3
Connector #2 Pins B10/C10	PHY_SW3_ TXN/TXP	OUTPUT, SERDES, 100 ohm differential	SERDES Transmit Ethernet diff-pair signal from CMM to Ethernet Switch #3
Connector #2 Pins D1	SMB_PSU_SCK	OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Power Supplies in system. 5V TTL level signal.
Connector #2 Pins E1	SMB_PSU_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector.	I2C Bus for Power Supplies in system. 5V TTL level signal.
Connector #2 Pins E2	SMB_FAN_SCK	OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Fan Modules used in system. 5V TTL level signal.
Connector #2 Pins F2	SMB_FAN_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Fan Modules used in system. 5V TTL level signal.
Connector #2 Pins D3	SMB_I/O_SW1_SCK	OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for I/O and Switch module section #1. 5V TTL level signal.
Connector #2 Pins E3	SMB_I/O_SW1_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for I/O and Switch module section #1. 5V TTL level signal.
Connector #2 Pin E4	FM_SDCD_FLSH_ CLK	OUTPUT, 10K pullup to 3.3 V on mid-plane.	SD Card Storage interface, CLOCK Line. LVTTL level signal.
Connector #2 Pin F4	FM_SDCD_FLSH_ CMD	OUTPUT, 10K pullup to 3.3 V on mid-plane.	SD Card Storage interface, COMMAND Line. LVTTL level signal.
Connector #2 Pins D5	SMB_BL_1_SCK	OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Blade I2C Bus #1 (interface to blades #1, #2, #3). 5V TTL level signal.
Connector #2 Pins E5	SMB_BL_1_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Blade I2C Bus #1 (interface to blades #1, #2, #3). 5V TTL level signal.
Connector #2 Pin E6	FM_SDCD_FLSH _PW-RST	Output, pulled up to 3.3 V on Midplane, Open collector output	Pulled low, this powers on the SD flash card. To reset the card, release this line for 250ms, then reapply (low) and wait 500ms before accessing SD Card memory.

Pin Number	Signal Name	Signal Type & Polarity	Description / Definition
Connector #2 Pin F6	CMM_PWR_ON	INPUT, 12 V DC input to the Hot Swap controller for startup.	+12 V DC power for short pin input to hot swap controller startup.
Connector #2 Pins D7	SMB_BL_2_SCK	OUTPUT, 5V Pullup on mid-plane, Open Collector output.	I2C Bus for Blade I2C Bus #2 (interface to blades #4, #5, #6). 5V TTL level signal.
Connector #2 Pins E7	SMB_BL_2_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Blade I2C Bus #2 (interface to blades #4, #5, #6). 5V TTL level signal.
Connector #2 Pins E8	SMB_BL_3_SCK	OUTPUT, 5V Pullup on mid-plane, Open Collector output.	I2C Bus for Blade I2C Bus #3 (interface to blades #7, #8, #9, #10). 5V TTL level signal.
Connector #2 Pins F8	SMB_BL_3_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane. Open Collector output.	I2C Bus for Blade I2C Bus #3 (interface to blades #7, #8, #9, #10). 5V TTL level signal.
Connector #2 Pin G1	FM_BL1_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #1 Compute Blade Module position.
Connector #2 Pin H1	FM_BL2_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #2 Compute Blade Module position.
Connector #2 Pin H2	FM_BL3_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #3 Compute Blade Module position.
Connector #2 Pin I2	FM_BL4_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #4 Compute Blade Module position.
Connector #2 Pin G3	FM_BL5_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #5 Compute Blade Module position.
Connector #2 Pin H3	FM_BL6_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #6 Compute Blade Module position.
Connector #2 Pin H4	FM_BL7_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #7 Compute Blade Module position.
Connector #2 Pin I4	FM_BL8_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #8 Compute Blade Module position.
Connector #2 Pin G5	FM_BL9_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #9 Compute Blade Module position.
Connector #2 Pin H5	FM_BL10_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Present detect into the CMM from the #10 Compute Blade Module position.
Connector #2 Pin H6	FM_SDCD_FLSH_DAT_2	INPUT/OUTPUT, 10 k pullup to 3.3 V on mid-plane.	SD Card Storage interface, Data line 02. LVTTL level signal.
Connector #2 Pin I6	FM_SDCD_FLSH_DAT_3	INPUT/OUTPUT, 10 k pullup to 3.3 V on mid-plane.	SD Card Storage interface, Data line 03. LVTTL level signal.
Connector #2 Pin G7	FM_SDCD_FLSH_DAT_0	INPUT/OUTPUT, 10 k pullup to 3.3 V on mid-plane.	SD Card Storage interface, Data line 00. LVTTL level signal.
Connector #2 Pin H7	FM_SDCD_FLSH_DAT_1	INPUT/OUTPUT, 10 k pullup to 3.3 V on mid-plane.	SD Card Storage interface, Data line 01. LVTTL level signal.
Connector #2 Pins H8	SMB_I/O_SW2_SCK	OUTPUT, 5V Pullup on mid-plane, Open Collector output.	I2C Bus for I/O and Switch module section #2. 5V TTL level signal.
Connector #2 Pins I8	SMB_I/O_SW2_SDA	INPUT/OUTPUT, 5V Pullup on mid-plane, Open Collector output.	I2C Bus for I/O and Switch module section #2. 5V TTL level signal.
Connector #2 Pin J1	FM_FAN1_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #1 Present sense line. LVTTL level signal.
Connector #2 Pin K1	FM_FAN2_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #2 Present sense line. LVTTL level signal.
Connector #2 Pin K2	FM_FAN3_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #3 Present sense line. LVTTL level signal.

Pin Number	Signal Name	Signal Type & Polarity	Description / Definition
Connector #2 Pin L2	FM_FAN4_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #4 Present sense line. LVTTL level signal.
Connector #2 Pin J3	FM_FAN5_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #5 Present sense line. LVTTL level signal.
Connector #2 Pin K3	FM_FAN6_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Fan Module #6 Present sense line. LVTTL level signal.
Connector #2 Pin K4	FM_PS1_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #1 Present sense line. LVTTL level signal.
Connector #2 Pin L4	FM_PS2_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #2 Present sense line. LVTTL level signal.
Connector #2 Pin J5	FM_PS3_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #3 Present sense line. LVTTL level signal.
Connector #2 Pin K5	FM_PS4_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #4 Present sense line. LVTTL level signal.
Connector #2 Pin K6	FM_PS5_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #5 Present sense line. LVTTL level signal.
Connector #2 Pin L6	FM_PS6_PRES_N	INPUT, Pullup to 3.3 V on mid-plane.	Power Supply #6 Present sense line. LVTTL level signal.
Connector #2 Pin K7	FM_CM_SLOT_ID	INPUT, Pullup to 3.3 V or Pulldown to GND on mid-plane	CMM Slot ID#0 (ADDR_0) Set Input (set by chassis pullup/pulldown). LVTTL level signal.
Connector #2 Pins: J7,K8,L8, D9,E9,G9,H9,J9, K9,E10,F10,H10, I10,K10,L10	RESERVED	Reserved, undefined signal pin.	Signal pin reserved for future design needs.
Connectors #1 & #2: A2,A4,A6,A8,A10, C1,C3,C5,C7,C9, D2,D4,D6,D8,D10 F1,F3,F5,F7,F9 G2,G4,G6,G8, G10,I1,I3,I5,I7,I9 J2,J4,J6,J8,J10 L1,L3,L5,L7,L9	GND	DC Power and Signal Ground.	System and circuit ground.

Table 2-3: Mid-plane Connector Signal Type Definition

Signal Type	Description / Definition
GND	Signal and Power Ground.
Power	+12 V DC power from mid-plane.
PHY	10/100 SERDES signals to an Ethernet switch.
FM_SDCD_FLSH_CLK/ CMD/DAT_[0..3]	Reserved for SD Card Flash device interface. SD card to be located on system mid-plane for data and software image storage.
SMB	Management I2C Control bus.
_CLK	I2C Bus Clock.
_DAT	I2C Bus Data.
SMB_BLx_CLK/DAT	Blade I2C bus #x (split into 3 groups for I2C loading control).
SMB_PSU_CLK/DAT	Power Supply I2C Group – Single bus just for power supplies.
SMB_FAN_CLK/DAT	Fan I2C Bus – Single bus for all FAN modules.

Signal Type	Description / Definition
IO_SWx_CLK/DAT	I/O and Switch module I2C bus #x (split into two busses for loading control).
FM_	Static management detection signals.
FM_PRES_N	"Module Present" signal indicating presence of module to CMM; pulled low for module present.
FM_BL_x_SPARE	Signals reserved between the CMM and Compute Blade that can be routed on the mid-plane for un-anticipated control/communications signals.
FM_CM_SLOT_ID	Set Slot Address for the CMM.
CMM_PWR_ON	P12V connection into the Hot-Swap controller to turn on the power into the CMM. This is the "Short Pin" in the connector so that power and ground are connected before the Hot-Swap controller is enabled.
FM_BL_x_ SPARE	Spare connection for each blade from CMM.
FM_SW_I2C_INT_A/B	Interrupt line from the switches to the CMM to interrupt the I2C port in the event that the switch wants to become bus master.
FM_I2C_RESET_N	Reset line from the CMM to reset all the I2C controllers on the bus. This line is true LOW.
FM_CMM_SELECT_A/B_N	Active (master) CMM select line for the system modules. This line is LOW TRUE for the master CMM, and HIGH for the standby module.
SPARE_CMM-CMM	Signals reserved for additional CMM to CMM signaling/communications lines.
RESERVED	Reserved for future needs.

2.3.3 CMM Power Connections

The power connection for the CMM is provided through the signal connector using ten of the connector pins to provide a minimum of 5 amps of 12 V. The thermal limit for power in the CMM is set at 50 Watts.

Connector #1, Pins E10, F10, G9, H9, H10, I10, J9, K9, K10, L10 are used for 12 V input to the CMM.

3 CMM Electrical Signal Considerations

3.1 Management Ethernet Signal Routing

Lengths for PHY signals (10/100 SERDES) should be monitored for good design practices within the system design.

3.2 I2C Bus Implementation

3.2.1 Operating Voltage

The system I2C operating voltage **shall** be 5V.

3.2.2 System Pullups

System pullup resistors **shall** be located on the system mid-plane board for all of the I2C busses in the system.

- It is recommended that the minimum value of pullup supported by the I2C specification be used to keep the rise-time of the signal as fast as possible
    - A 4.7 k ohm resistor is the maximum value recommended for 100 kHz operation with a maximum bus capacitance of 400 pF. It is recommended to carefully evaluate your system design and use a value of pullup that is compliant with the devices used on the bus, and one that affords the desired response time to meet 100 kHz bus operation.
    - See I2C bus specification Version 2.1, or later, for definition of requirements for 100 kHz operation.

3.2.3 I2C Operating Frequency

The operating frequency of the I2C bus **shall** be 100 kHz.

3.2.4 I2C Arbitration and Control

In order to support dual CMMs and the likelihood of a failover scenario between the two modules, there needs to be a method to select the CMM with an I2C bus controller that is operating properly should a module failure occur. Dual I2C busses are used throughout for SSI chassis control. For this reason, a method that provides assurance of operation on the bus by ONLY the functioning CMM was chosen, using the arbitration logic method.

To make sure the primary CMM is the only one that can communicate on its I2C bus, the output FPGA (or other device – this output control could be done using a CPLD) should control the CMM I2C bus output, the I2C Reset line, and

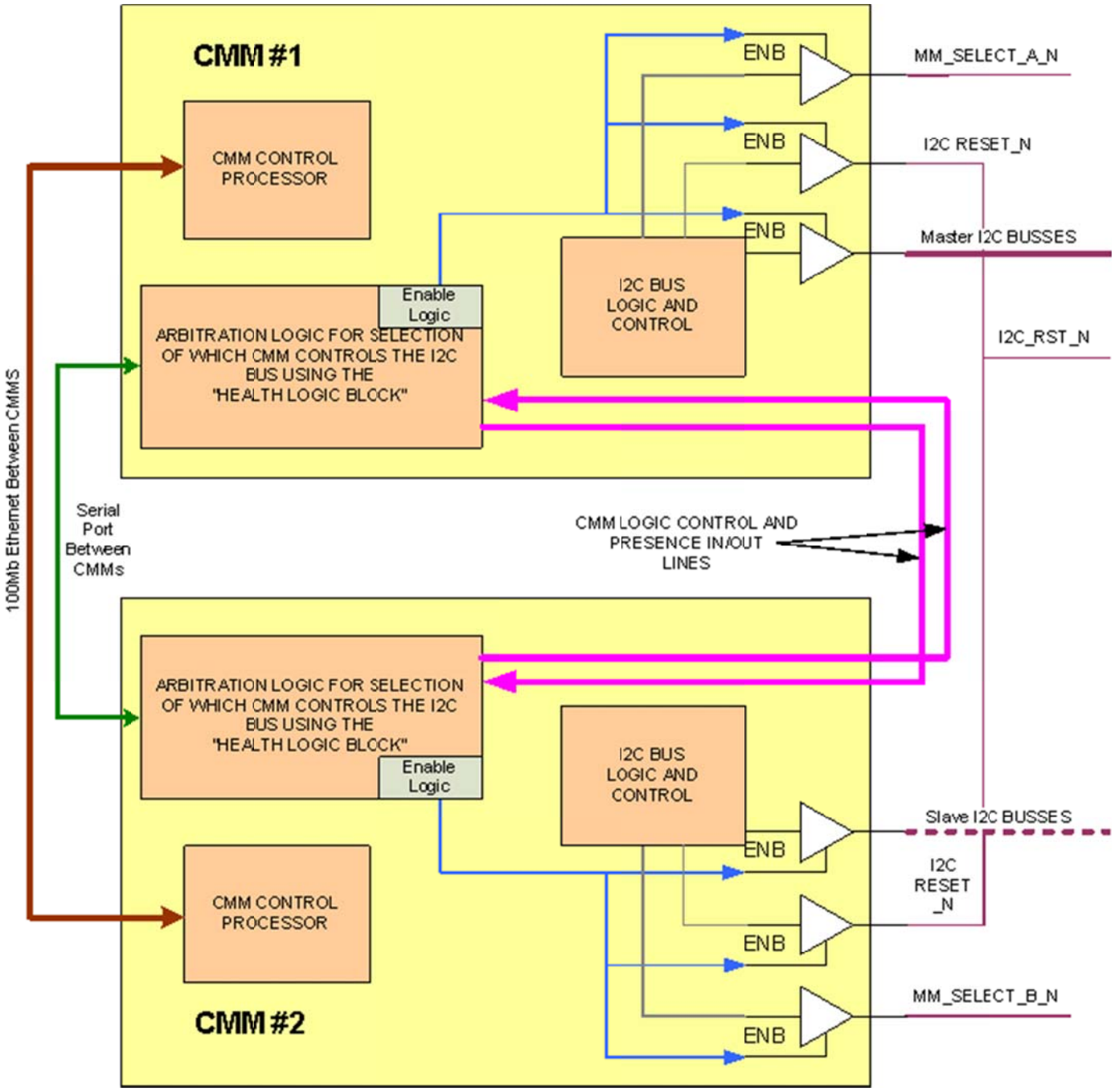
the CMM select lines used by the SSI switches. By using a system of logical pulses as the controlling input to the I2C output control device for selection, it could be set up so that ONLY the primary CMM would be controlling the I2C bus output. To implement this in the output device, the heartbeat and control software between the two CMMs will decide which is the primary CCM and which is in standby mode. The controlling CMM (primary) will send a data byte to the control register of the standby CMM output device. The output device decodes it as an enable or disable code for that output device. Communication between CMMs for enable/disable can be via the serial port or the 100 Mbps Ethernet that both operate between the CMMs.

Should a CMM be “dead”; i.e. VR failure; the output device should fail to either a high state, or a high impedance (tri-state) output condition, leaving that I2C bus in a non-active state.

The enable code for the output device can be any logical bit ordering of at least 8 bits. This provides a robust selection mechanism in determining which CMM is enabled to communicate on the I2C bus, and eliminates the possibility of both CMMs trying to communicate at the same time. In the event of a “hung” bus segment, the non-active CMM can be used to poll the devices on the bus to find which device is locking the bus, and alert the System Administrator that there is a problem and in which module the problem is located. There is also provision for an I2C reset line that can be used to reset the I2C modules throughout the chassis. This line is required for the SSI switch management, but it is optional if the system designer wants to implement this throughout the chassis.

See Fig 3-1 for a diagram of the concept.

Figure 3-1: I2C Arbitration and Control Diagram



In this diagram, the enable logic, driven from the Arbitration Logic block, would receive a control byte to set the enable lines for the I2C bus, MM_SELECT_A/B_N, and I2C RESET_N lines output control. Without the correct bit sequence, the enable logic would not be set. This prevents a CMM that has failed (either hardware or firmware) and is out of control, from controlling and driving the I2C bus.

3.2.5 Bus Driver Capability

The output drivers for the I2C bus controller should be scalable in output drive current in order to better control undershoot, overshoot, and other system noise problems.

3.2.6 Use of Repeaters and "I2C Buffers"

It is recommended to avoid so-called I2C buffers and repeaters in the system design. These components can frequently cause spurious operation of the I2C bus, causing bus contention and missed or corrupted data.

3.3 I2C Bus Loading

3.3.1 Division of Busses in the System Design

It is recommended that the I2C busses in the system be divided in a manner that keeps the distributed capacitance on each of the busses at a minimum.

For instance, the signal connectors define two specific I2C (SMB) busses for the I/O modules (switches and custom I/O). If these are divided in the system architecture such that the loading of each of these busses is about the same with a full loading of I/O modules, performance will be optimized.

It is HIGHLY STRESSED that care be taken in the design of the I2C busses for system management, such that they are not overloaded to prevent communications problems.

3.3.2 Number of inputs per bus

The number of device inputs per bus **shall** be controlled to ensure that bus capacitance loading is maintained within the I2C bus specification (about 400 pF).

3.3.3 Trace Route Length Concerns

Trace routing lengths should be monitored in the system such that the distributed capacitance, combined with the number of inputs per bus, does not exceed the I2C bus capacitance loading specification of 400 pF maximum.

4 CMM Power Control

4.1 Input Power Requirements

Input power to the CMM is accomplished through the signal connector as outlined in section 2.3.3 above.

The required power for the CMM is derived from the system 12 V supply provided from the system mid-plane. This voltage should conform to the system 12 V requirements.

4.2 Hot Swap Requirements

All modules in a blade server system should be hot-swappable; meaning they should be able to be removed and re-inserted while the system is running in a normal mode, with no negative impact on the system operation. To accomplish this, a hot-swap controller must be used for each module, which **shall** assure the input current surge current to the module is controlled in a “soft start” fashion.

Overcurrent protection **shall** also be provided (usually this is an ancillary function of the hot-swap controller) to ensure that a defective module is removed from the internal power distribution grid, and will not overload the system 12 V to protect the system from failure or shutdown.

4.3 Power Sequencing Requirements

As mentioned above, the CMM itself **shall** power up in a soft start controlled fashion to prevent high current surges from disrupting system operation during hot insertion.

Power sequencing for the CMM internal circuitry should be implemented as the internal components require. It is left to the individual implementer to accomplish in the manner necessary for the circuit components chosen.

4.4 Overcurrent Protection Limit

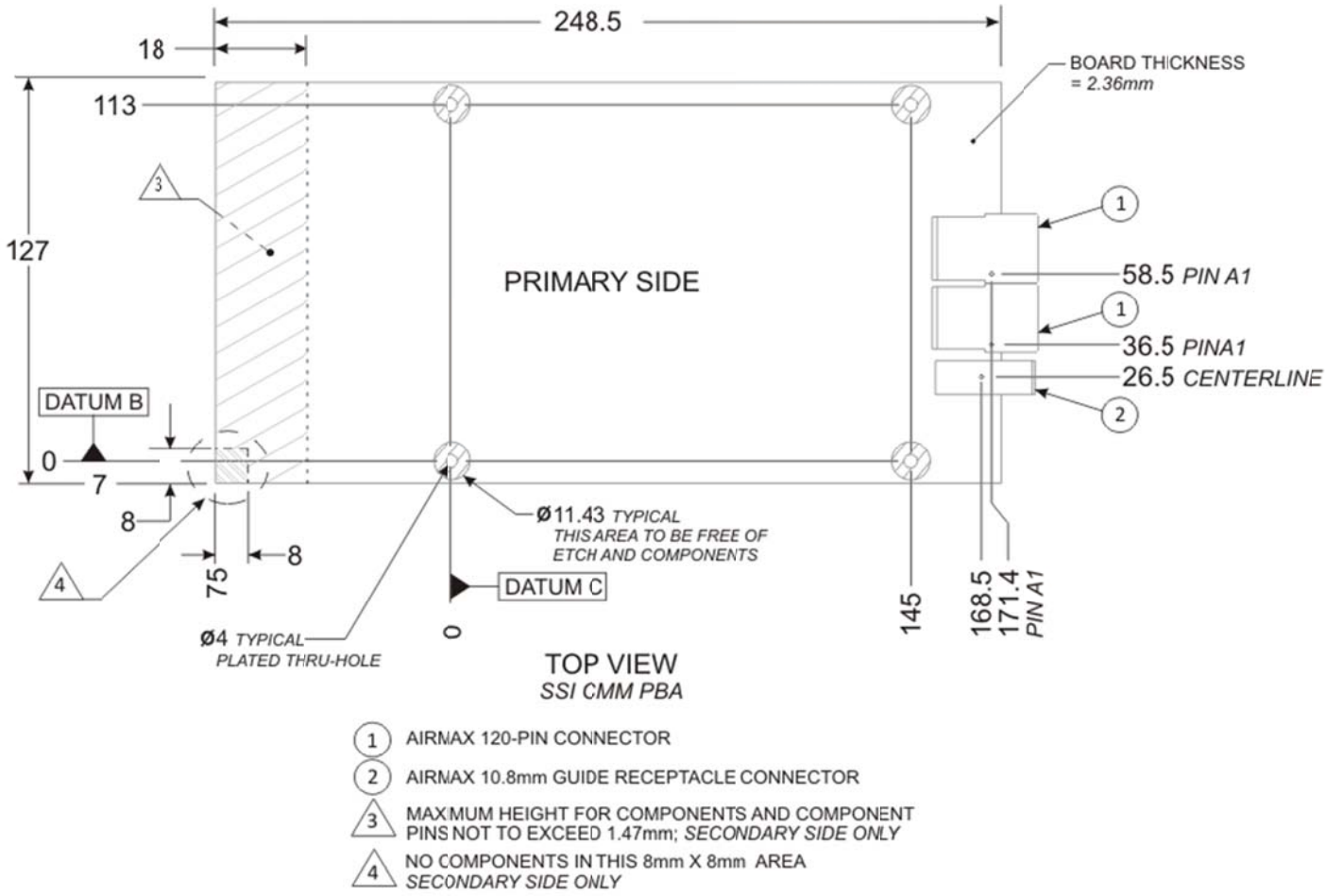
Overcurrent protection **shall** be provided to limit the maximum current in the CMM to 150% of maximum power. Maximum power is defined above as 50 Watts, therefore overcurrent protection **shall** limit input current from the 12 V system bus to a maximum level of approximately 6.25 amps (about 75 W).

5 CMM PBA Mechanical Specifications

5.1 CMM PBA Mechanical Dimensions

The CMM PBA is 248.5mm long by 127mm wide.

Figure 5-1: PBA Mechanical Drawing



5.2 CMM PBA Mechanical / Thermal Guidelines

The maximum power level for the CMM is 50 W.

5.2.1 CMM Component Height Limitations

Suggested Maximum height for components is 20.34 ± 0.34 mm

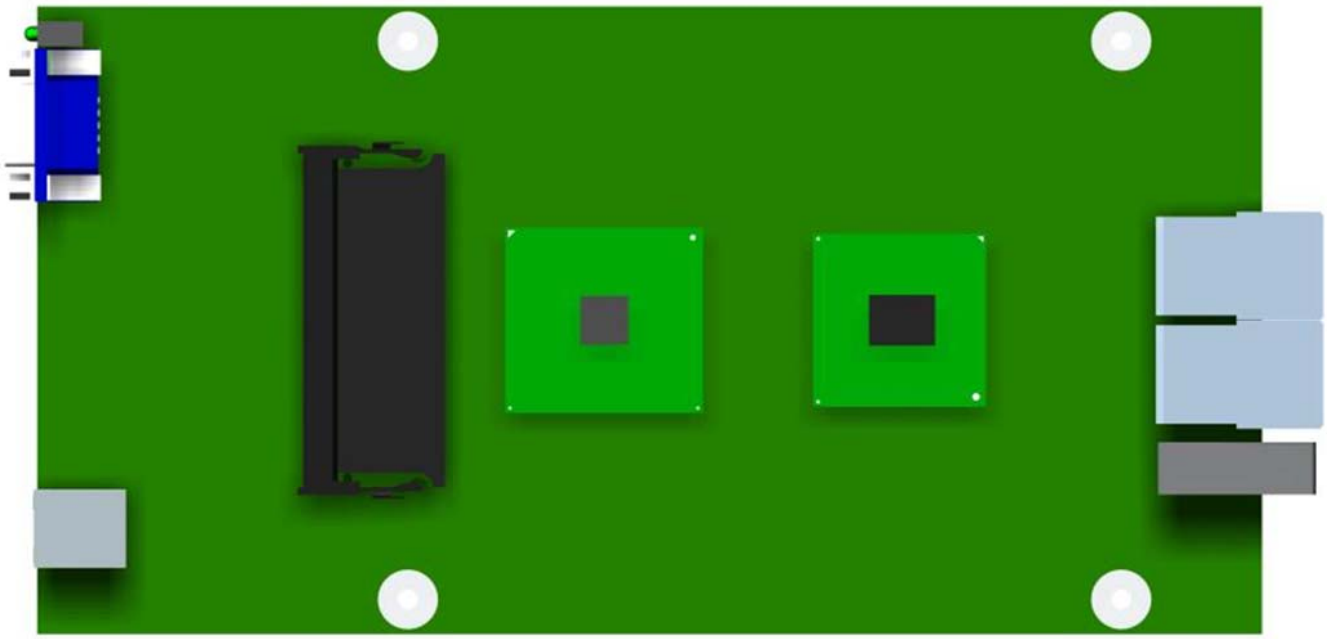
5.2.2 CMM PBA Connectors

The signal connectors used for the CMM to mid-plane interface are two 120-pin (4-Pair) Airmax connectors. The proper PN for this connector that will be used on an SSI module is listed in Table 2-1.

5.3 CMM PBA

Below is a sample placement of the major components for the CMM PBA. The only components that are fixed in position are the mid-plane interface connectors and guide pin. Other components are up to the module developer.

Figure 5-2: Sample Component Placement



6 CMM Thermal Management

6.1 Introduction

Airflow requirements (and limitations) for the CMM are determined by several factors including but not limited to the following: total heat dissipated, component selection, component density, component location, heat dissipation per device, acoustic targets, and practical limits of forced air cooling technology.

No general specification can dictate exactly how to adequately cool an unknown design, but general guidelines are presented herein. This specification is intended to enable air cooling of a wider variety of forward looking components.

6.1.1 CMM Thermal-Airflow Needs

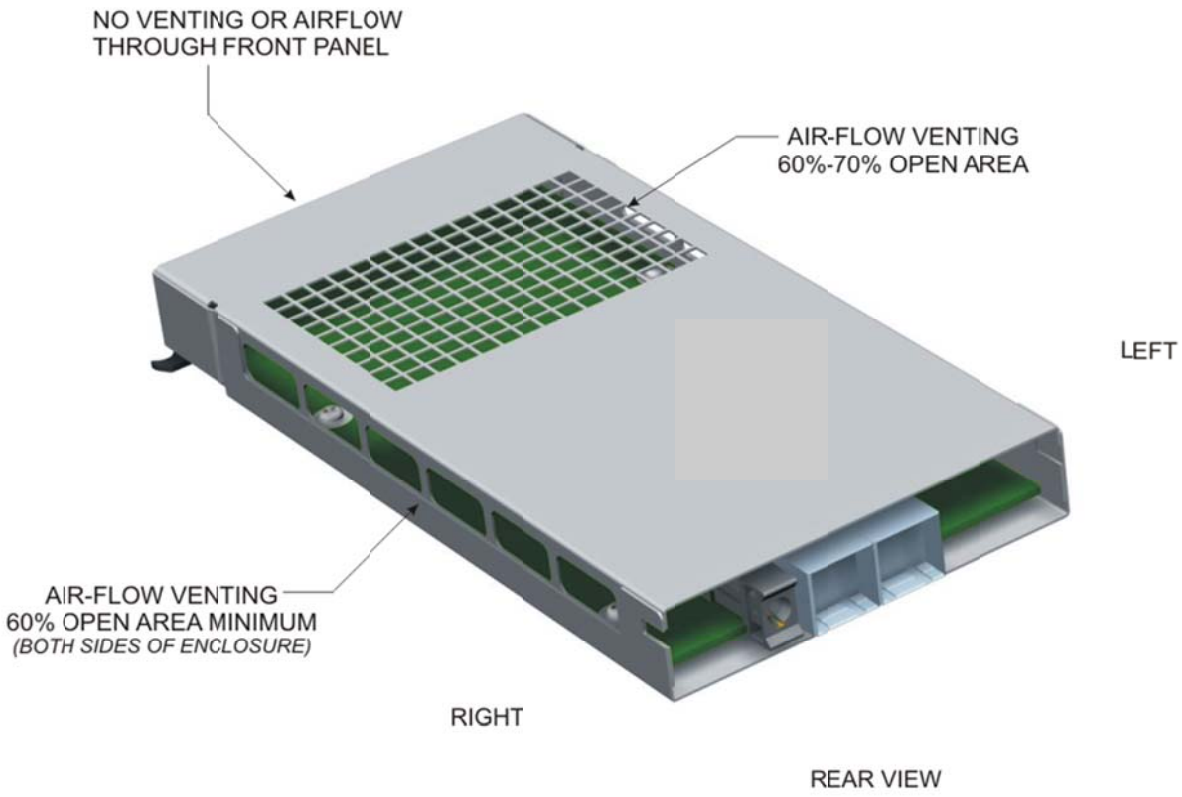
The CMM can be installed into chassis with differing designs that conform to the SSI specification; therefore, multiple airflow paths and local ambient temperatures need to be considered when designing and determining the thermal solution.

Airflow can be one of the following:

- 1: left to right
- 2: right to left
- 3: rear to top
- 4: side to top
- 5: rear to side(s).

See Figure 6-1 below.

Figure 6-1: Module Airflow Description



The expected worst-case ambient air temperature entering the CMM in performance condition is 51° C.

The expected worst-case ambient air temperature entering the CMM in acoustic mode is 46° C.

System integrators and designers will be expected to deliver a minimum of 15 CFM in a performance state.

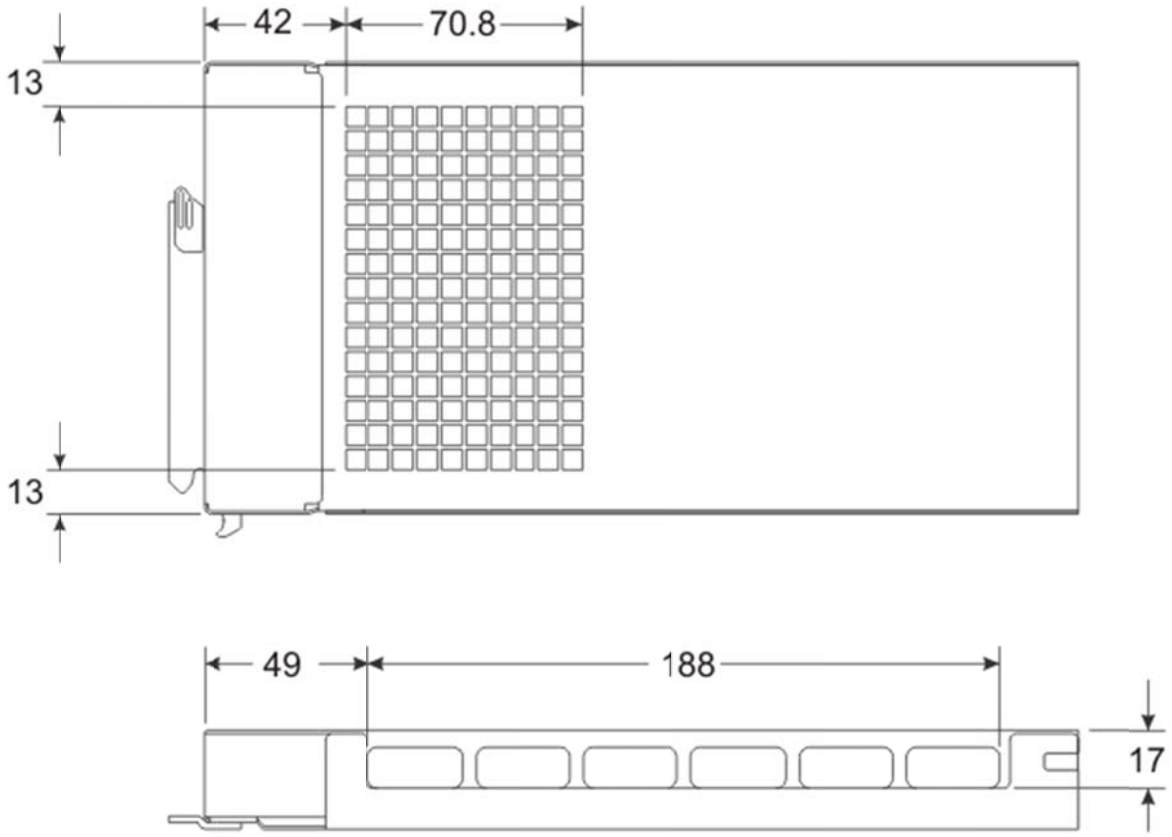
System integrators and designers will be expected to deliver a minimum of 10 CFM in an acoustic state.

The thermal design will need to consider flow rates, air flow distributions, and ambient temperatures when designing and verifying the CMM cooling solution.

6.1.2 Mechanical Enclosure Venting Requirements

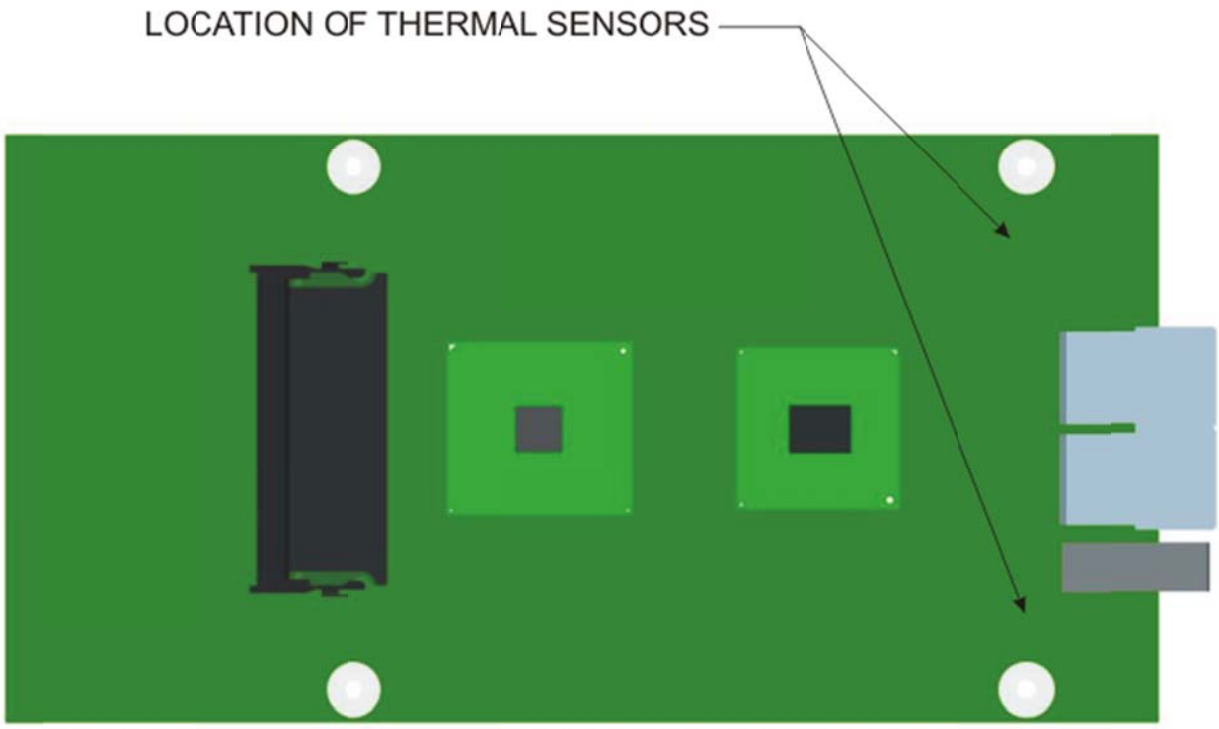
Figure 6-2 describes the venting required to allow sufficient airflow through the CMM. All defined venting is required, such that all SSI compliant air flow paths are supported. Chassis solutions, at the discretion of system developers, may or may not leverage all required CMM enclosure venting to achieve proper cooling.

Figure 6-2: Enclosure Mechanical Venting



Two local ambient temperature sensors are to be located approximately where shown in Figure 6-3. System designers and integrators will need to characterize these temperature sensors for their particular implementation.

Figure 6-3: Location of Thermal Sensors



NOTE: Issue 304 removed previous chapter 7: Environmental Requirements.

7 Shock / Vibration Requirements

7.1 Requirements

Shock and vibration test levels for the CMM is defined in this section. It is recommended that tests at both the module level and product level be performed. However, in cases where this is not practical, CMM testing using a rigid chassis test fixture as described below is, in most cases, acceptable.

Testing of the CMM **shall** be unpackaged, packaged, and in a chassis when practical (fully loaded chassis unpackaged, packaged, and in a rack).

Note: For telecom environments, the CMM must abide by Telcordia GR-63-CORE, Issue 3 for shock & vibration requirements.

- Section 4.3.1: Packaged Shock
- Section 4.3.2: Unpackaged Shock
- Section 4.4.1: Earthquake Zone 4
- Section 4.4.3: Office Vibration
- Section 4.4.4: Transportation Vibration

Refer to GR-63-CORE Section 5 for associated test methods.

7.2 Pass / Fail Criteria

The product **shall** be inspected for mechanical damage after each test. Any noticeable damage is considered a failure. The product **shall** be operated before and after each test using an operating system and test exercise program to ensure it functions as designed.

7.3 Test Fixture

7.3.1 Operational Tests

For operational tests, the SSI chassis under test **shall** be clamped to the test table with rigid fixtures that support the chassis in a manner that simulates the support provided by the intended shipping package. Rack-level operational vibration and shock testing is not performed.

7.3.2 Non-Operational Tests

For non-operational tests, the product **shall** be supported and clamped to the test table in a manner that simulates the support provided by the intended shipping package. For example, a CMM should be installed in a chassis that is clamped to the test table with rigid fixtures that support the SSI chassis at the same locations as found in the shipping package.

If an SSI chassis is not available, a rigid chassis test fixture for the CMM may be used. This fixture **shall** be a rigid structure designed to simulate the support

and retention mechanisms of an SSI chassis. This structure should have a natural frequency of greater than 200 Hz. It **shall** provide the same guide channels, latch retention, and connector system as a chassis. The signal and power connectors should be mounted on a board or other structure that will simulate the SSI mid-plane.

7.4 Operational Shock and Vibration

The following operational shock and vibration tests **shall** be performed on a test table. The tests are not performed in a rack.

7.4.1 Operational Shock

CMM on, operational shock:

- Vertical Input: 30.0 G for 3 ms, half-sine shock pulse.
- Horizontal Input: 15.0 G for 3 ms, half-sine shock pulse.
- Two shock inputs in each axis, one in each direction; six total.

7.4.2 Operational Vibration

CMM on, operational vibration: 0.27 G RMS at 5 Hz to 500 Hz for 30 minutes.

Power Spectral Density (PSD) for operational vibration tests is provided in Table 7-1.

Table 7-1: Random Vibration PSD Profile for Chassis and CMM Operational Unpackaged Test

Frequency	G^2 / Hz (PSD Level)
5.0	2.0×10^{-5}
17.0	3.0×10^{-4}
45.0	3.0×10^{-4}
48.0	3.0×10^{-4}
62.0	3.0×10^{-4}
65.0	3.0×10^{-4}
150.0	3.0×10^{-4}
200.0	8.0×10^{-5}
500.0	8.0×10^{-5}

7.5 Non-operational Shock and Vibration

Non-operational chassis and CMM vibration and shock test levels are defined below. Chassis level tests **shall** be performed with and without blades. In each case, the chassis **shall** be fully populated with modules. Chassis tests **shall** be performed using shock and vibration test tables and in a rack. It is intended that the CMMs be tested as individual units and in the chassis. However, for companies developing CMMs, an alternate test method is to use a rigid test fixture as described above, and test only to CMM levels. This test method will result in a reasonable assurance that failure will not occur. However, if practical, it is recommended that chassis level testing be performed.

7.5.1 Non-operational Fragility Random Vibration

Unpackaged (fragility) random vibration tests are performed in accordance with levels in Table 7-2. If the product fails during random vibration testing, additional sinusoidal vibration and dwell testing **shall** be used to determine weak areas of the product. The sinusoidal test **shall** consist of a sweep at 0.5 G from 2 Hz to 200 Hz to determine the most dominant natural frequency, and then dwell at the natural frequency for 15 minutes. Once improvements are made to the design, the unpackaged random vibration tests **shall** be re-run to ensure compliance to the test levels.

Table 7-2: Non-operational Unpackaged - CMM

Orientation	GRMS	Duration (minutes)
Bottom	1.463	15
Top	1.463	15
Right	1.463	15
Left	1.463	15
Front	1.463	15
Rear	1.463	15

The random vibration test spectrum for non-operational, unpackaged testing **shall** be in accordance with Table 7-3.

Table 7-3: 1.463 GRMS Random Vibration Spectrum for Chassis and CMM Tests

Frequency	G^2 / Hz (PSD Level)
2.0	0.0010
4.0	0.0300
8.0	0.0300
40.0	0.0100
200.0	0.0100

7.5.2 Non-Operational Fragility Shock – Unpackaged CMM

Unpackaged CMM shock test levels are defined in Table 7-4.

CMMs may be qualified using a rigid chassis test fixture, as described in the test fixture section of this document, in lieu of the chassis-level test described in the section above. The levels in Table 7-4 **shall** be used to test CMMs in the rigid chassis test fixture.

Table 7-4: Non-Operational Unpackaged CMM Shock Test Levels

Orientation	G's	Delta-V mm/sec (in./sec)	Wave Form
Bottom	50	4,572 (180)	Trapezoid
Top	50	4,572 (180)	Trapezoid
Right	50	4,572 (180)	Trapezoid
Left	50	4,572 (180)	Trapezoid
Front	50	4,572 (180)	Trapezoid

Rear	50	4,572 (180)	Trapezoid

7.5.3 Non-operational, Packaged Random Vibration

Packaged random vibration tests are performed in accordance with levels in Table 7-5. These levels are for the CMM Modules.

Table 7-5: Non-operational, Packaged – CMM

Orientation	GRMS	Duration (minutes)
Top or Bottom	1.463	15
Right or Left	1.463	15
Front or Rear	1.463	15

The random vibration test spectrum for non-operational, unpackaged testing **shall** be in accordance with Table 7-3.

7.5.4 Non-operational Shock – CMM

Table 7-6 lists the drop heights for specific weight ranges to be used to test packaged CMMs. Product acceleration response inside the package must be monitored during the test. The response must be lower than the unpackaged fragility acceleration target.

Table 7-6: Non-operational, Packaged CMM Drop Test Levels

Orientation	Drop Height mm (inches) Weight < 9.1 kg (20 lbs)	Drop Height mm (inches) Weight = 9.1 kg (20 lbs) to 18.2 kg (40 lbs)	Drop Height mm (inches) Weight = 18.2 kg (40 lbs) to 36.4 kg (80 lbs)
Bottom	914 (36)	762 (30)	610 (24)
Top	914 (36)	762 (30)	610 (24)
Right	914 (36)	762 (30)	610 (24)
Left	914 (36)	762 (30)	610 (24)

Front	914 (36)	762 (30)	610 (24)
Rear	914 (36)	762 (30)	610 (24)
Critical Corner	914 (36)	762 (30)	610 (24)
Critical Edge	914 (36)	762 (30)	610 (24)

8 Product Regulations Requirements

The CMM **shall** meet regulatory requirements as governed by specific country regulations.

9 Chassis IDROM

9.1 Midplane IDROM Device

A midplane [274] PBA shall provide a 5V tolerant I2C Serial EEPROM of type 24C64 (or compatible) that is capable of 100 kHz operation at a minimum, and shall be inter-operable with 400 KHz devices.

This device shall be connected to CMM SMB_SPARE I2C Bus.

This device shall be at I2C addresses ACh/ADh for read/write operations (56h + r/w bit). The device shall be powered via standby power.

This device shall be writable via I2C. This will enable the use case of Asset Tag and End Product information as well as firmware updates to the data structures.

9.2 IPMI FRU Inventory Support

The *IPMI v2.0* specification defines Field Replaceable Unit (FRU) Information commands and formats for querying and retrieving Inventory information from an IPMI capable entity. The *Intelligent Platform Management FRU Information Storage Definition v1.0 r1.1* specification defines the common format and use of the FRU Information using IPMI.

Independent of the mezzanine management model, the mezzanine PBA shall support IPMI FRU Inventory data which shall, minimally, contain the following areas:

- Common Header Area: This area contains pointers into the other IPMI FRU data areas.
- Chassis Info Area: The *Chassis Type (value = 1Dh)*, *Chassis Part Number* and *Chassis Serial Number* fields shall be supported. This area shall identify the chassis in the context of the the actual enclosure of the Chassis.
- Board Info Area: The *Mfg Date/Time, Manufacturer, Product Name*, *Serial Numbe, and Part Number* fields shall be supported. This area shall reflect the information in the context of the Chassis Midplane.
- Product Info Area: The *Manufacturer, Product Name, Part/Model Number, Version and Serial Number* fields shall be supported. This area shall reflect the information in the context of the entire system configured as a end product. Different system configurations (if packaged as different products) may have unique information in this area. This is typically the information the end customer would see to identify the entire system.
- MultiRecord Area: This area shall contain a SSI Chassis General Record, a Slot Record for each chassis slot, a Supplemental IO Record for each Switch/IO slot, and an OEM Form Factor Record for each Non-SSI form factor listed in the Slot Record Table.

All area and record checksums shall be correctly maintained.

Additional Multi Record Entries may be supported at the manufacturer's discretion.

All multibyte values (such as uint16 or uint24) shall be encoded as Little Endian (LSB First).

All array's are indicated with [] and shall be encoded with the number of bytes indicated within the brackets.

9.3 MultiRecord Area SSI Records

The General FRU area is described in the IPMI FRU specification, therefore the Common, Chassis, Board, and Product areas will not be covered in detailed in this specification. The General layout of the Multirecord area (populated with SSI Records) is in the following table.

Table 9-1: SSI FRU Multirecord Area

Offset	Size	Description
0	43	Chassis General Record GUID and Basic Chassis Capacities
43	17*x	Slot Records[x] Each slot information, id and location
xxx	20*y	Extended Switch Records[y]
xxx	12*z	OEM Form Factors[z]
Total Length		43+17*x+20*y+12*z
Max Chassis	771	x=slot count, y=switch count, z=custom slot count

It is also worth noting in the preceeding table that a modeled chassis with all presence lines taken will use 771 bytes. This size is not guaranteed for any particular design and it is important that system designers perform their own calculations to determine the Muti-Area Size.

9.4 Chassis General Record

This record will generally identify the chassis GUID, capacities and information about the number of records following this record.

Table 9-2: SSI Chassis General Record

Offset	Type	Size	Description
0		1	Record Type ID C1h (OEM-SSI-Chassis) Shall Be Used
1		1	7:7 – End of list 6:4 – Reserved, write as 000b 3:0 – Record Format version (=2h unless otherwise specified)
2		1	Record Length = 48
3		1	Record Checksum
4		1	Header Checksum
5	uint8[16]	16	Chassis GUID Described in RFC 4122 Store as 16 Separate Bytes (msb0 first)
21-23	uint24	3	Manufacturer IANA Enterprise Number http://www.iana.org/assignments/enterprise-numbers LSB First.
24-25	uint16	2	Unique Product ID Provides a unique (within manufacturers domain) Product Type Identifier This field, in combination with the IANA number is here to give a reliable way to (programattically) uniquely identify the chassis type. These fields should not changed often and product facing names should be in the Product Info FRU Record.
26	uint8	1	Number of Compute Blade Slots
27	uint8	1	Number of Switch Slots
28	uint8	1	Number of SD Cards (1 or 2)
29	uint8	1	Number of Power Supply Slots
30	uint8	1	Number of Fan Module Slots
31	uint8	1	Number of CMM Module Slots
32	uint8	1	Number of Slot Records
33	uint8	1	Number of I/O Records
34	uint8	1	Number of Form Factor records
35	unit8	1	Chassis Height in Standard 1U Rack Units
36-37	unit16	2	Chassis Depth in mm
38-39	uint16	2	Width within rack (excluding ears) in mm (typical is 425mm)
40	uint8	1	Spec Compliance Version Major = 1
42	uint8	1	Spec Compliance Version Minor = 0
42	xxx	1	Reserved
Total Length		**43**	

9.5 Chassis Slot Records

Each chassis supports shall contain a Slot Record. These records provide addressing and physical information about all of the slots in the chassis. Please see the following Figure to understand the coordinate references in the table below:

Figure 9-1: SSI Chassis Reference Points

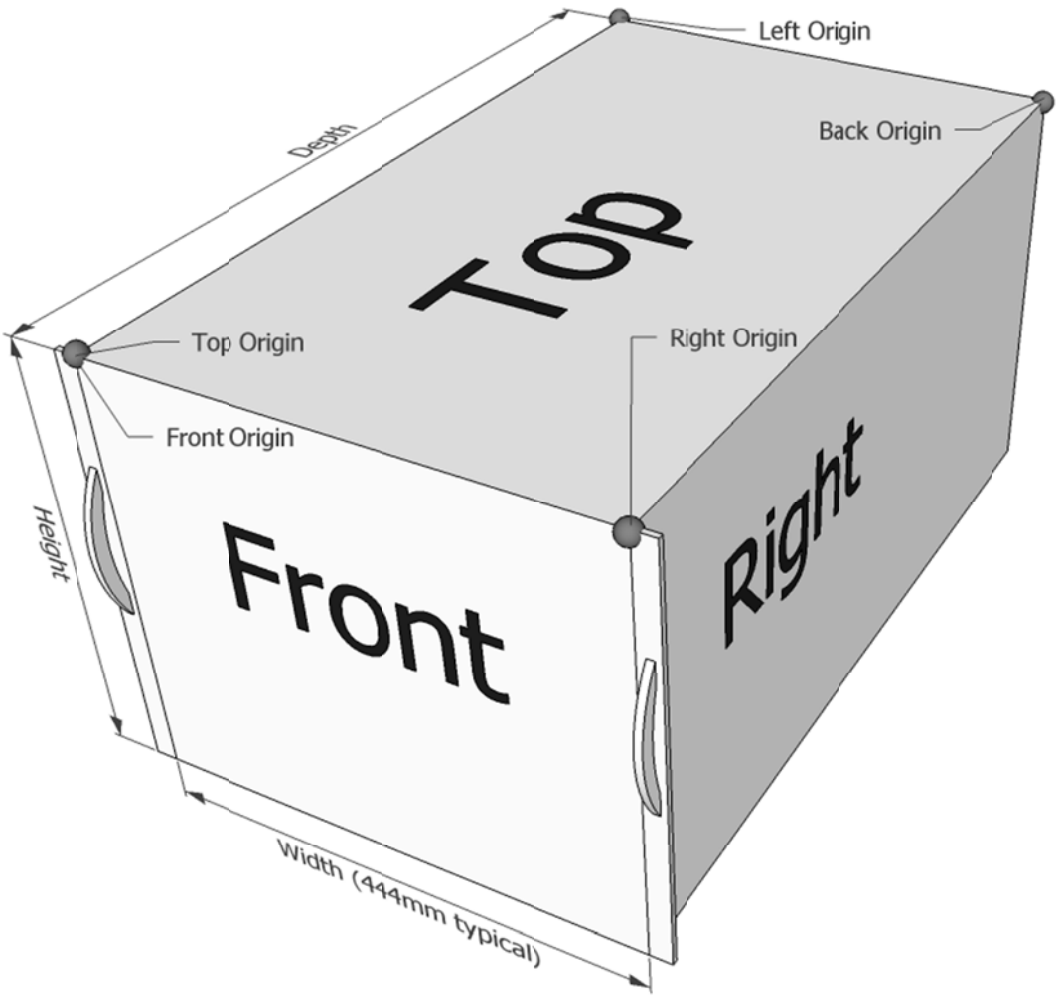


Table 9-3: SSI Chassis Slot Record

Offset	Type	Size	Description
0	uint8	1	Record Type ID C2h (OEM-SSI-Chassis-Slot) Shall Be Used
1	uint8	1	7:7 – End of list 6:4 – Reserved, write as 000b 3:0 – Record Format version (=2h unless otherwise specified)
2	uint8	1	Record Length =17
3	uint8	1	Record Checksum
4	uint8	1	Header Checksum
5	uint8	1	General Type of Slot 1 = Compute Blade Module 2 = I/O Switch Module 3 = Power Supply Module 4 = Fan Module 5 = Hard Drive Module 6 = Other
6	uint8	1	Presens\ce Line Wired to Slot None/CMM = 0 BL[1-10] = 1-10 SW[1-6] = 11-16 IO[1-2] = 17-18 FAN[1-6] = 21-26 PS[1-6] = 31-36 * Note, the presence lines must correspond with the external (paint) labeling of the module slots. Example: The presence line BL1 shall be routed to the slot on the chassis that is labeled as (Compute Blade) 1.
7	uint8	1	Slot Form Factor (implies Height/Width) 1=SSI Std Blade 2=SSI 1XSwitch 3=SSI 4X Switch 4=SSI CMM 5-100 Reserved 101-110 OEM Defined Form Factor
8	uint8	1	Slot ID Pins Blade 1-10 Should be 0-9

9	uint8	1	I2C Bus Number that Slot is on 0 = SMB_PSU 1 = SMB_FAN 2 = SMB_BL1 3 = SMB_BL2 4 = SMB_BL3 5 = SMB_SW1 6 = SMB_SW2 7 = SMB_RSVD 255 = None
10	uint8	1	I2C Address For Blades, the address shall conform to the Compute Blades specification in how the address relates to the Slot ID. For switches, this shall conform to the Definition in the Base Switch Spec. For non-SSI devices, this is a "convenience" field that may be used for determining the address of other devices within the chassis
11	uint8	1	Orientation and Face [7-4] - Reserved [3] - Orientation of largest dimension (Width) 0 = Vertical 1 = Horizontal [2-0] - Face of Chassis the slot is located 1 = Front 2 = Back 3 = Top 4 = Right (from Front) 5 = Left (from Front) * See Diagram for Face Locations
12-13	uint16	2	Slot Location X Horizontal Location with respect to Origin --left side of chassis (not including rack mount ears) Units = 1/10mm Value of 10 = 1mm * See Diagram For Origin Locations

14-15	uint16	2	Slot Location Y Vertical Location with respect to Origin - top of chassis Units = 1/10mm Value of 10 = 1mm
16	uint8	1	[7:6] - Reserved [5:4] - Provides Cooling 0 = No 1 = Yes 2 = Self Cooled/Does not cool other devices 3 = Self Cooled + cools other devices in zone (some power supplies fit this category) [3:0] - Cooling Zone for this device Zone 0 - 16 This field is used by both fans that service this zone and devices that are cooled within this zone Self Cooled Devices that do not cool other devices should use Zone 0. All other devices should be zone 1+
Total Length		**17**	

9.6 I/O Switch Supplemental Records

The primary purpose of these records are to provide an electrical capabilities profile for each slot as well as the port mapping for each slot. One record shall exist for each I/O Switch Slot.

Table 9-4: I/O Switch Supplemental Record

Offset	Type	Size	Description
0	uint8	1	Record Type ID C3h (OEM-SSI-IO-Supplemental) Shall Be Used
1	uint8	1	7:7 – End of list 6:4 – Reserved, write as 000b 3:0 – Record Format version (=2h unless otherwise specified)
2	uint8	1	Record Length = 20
3	uint8	1	Record Checksum
4	uint8	1	Header Checksum

5	uint16	1	Lane Compliance Bitmap of Channel communications standards supported Each bit should be on for each standard supported Bit Numbers xxxx xxxx xxxx xxxx fedc ba98 7654 3210 0 = KX 1 = KX4 2 = KR 3 = KR4 4 = DDR 5 = QDR 6 = 802.3ap 7 = FC4 8 = FC8 9 = PCIe - Gen1 a = PCIe - Gen2 b - f = Reserved
6-19	uint8[14]	14	Fabric Connect Table This is a Table that represents which internal ports on the switch connects to which blade ports The first byte implies port 1 on the switch, the second implies port 2, and so on... For Each Port, the byte is formatted as follows: bits 7:4 = Compute Blade Slot (1 - 10) bits 3:0 = Compute Blade I/O Fabric 0 = N/A 1 = Primary Fabric 1 2 = Primary Fabric 2 3 = Mezz Link 0 4 = Mezz Link 1 5 = Mezz Link 2 6 = Mezz Link 3 7 = Optional Fabric Link 0 8 = Optional Fabric Link 1
Total Length		**20**	

9.7 OEM Form Factor Records

For each non-standard (non-SSI) removable device form factor that is supported in the chassis such as fans, power supplies or other modules, a OEM Form Factor Record shall exist to describe the form factor. The form factor index in this table shall be referenced on non-SSI standard slot entries in the Slot Table (offset 7).

Table 9-5: SSI OEM Form Factor Record

Offset	Type	Size	Description
0	uint8	1	Record Type ID C4h (OEM-SSI-Chassis-OEMFF) Shall Be Used
1	uint8	1	7:7 – End of list 6:4 – Reserved, write as 000b 3:0 – Record Format version (=2h unless otherwise specified)
2	uint8	1	Record Length = 12
3	uint8	1	Record Checksum
4	uint8	1	Header Checksum
5	uint8	1	Form Factor ID Index of Form Factor: 101-110
6-7	uint16	2	Height Heigth of faceplate of module (smallest dimension) in 1/10 mm 10 = 1mm
8-9	uint16	2	Width Width of faceplate of module (largest dimension) in 1/10 mm
10-11	uint16	2	Depth Depth of module (not including connector) in 1/10 mm
Total Length		**12**	

A Appendix A: SSI CMM Thermal Design Guide – Thermal Management

A.1 Introduction

Airflow requirements (and limitations) for the CMM are determined by several factors, including, but not limited to: total heat dissipated, component selection, component density, component location, heat dissipation per device, acoustic targets, and practical limits of forced air cooling technology. The intent of this specification is to require a baseline air cooling solution for forward-looking designs. However, this baseline does not (and cannot) comprehensively address all previously mentioned design variables. In addition to ensuring that baseline conditions are satisfied, designers and integrators are encouraged to make sure that component- and/or module-level thermal requirements are met, given their own unique implementations.

A.2 Equipment Environment Specifications

All SSI-compliant systems are required to conform to ASHRAE TC9.9, Class 2. This module will be placed into an SSI-compliant system. Local ambient conditions for the CMM are determined by the chassis the CMM is being placed into and room ambient conditions. See Table 2.1 on page 10 of Reference ASHRAE “Thermal Guidelines for Data Processing Environments” ISBN 1-931862-43-5, Class 2, for blade system operating temperatures, humidity, and elevations.

A.3 CMM Thermal-Airflow Requirements

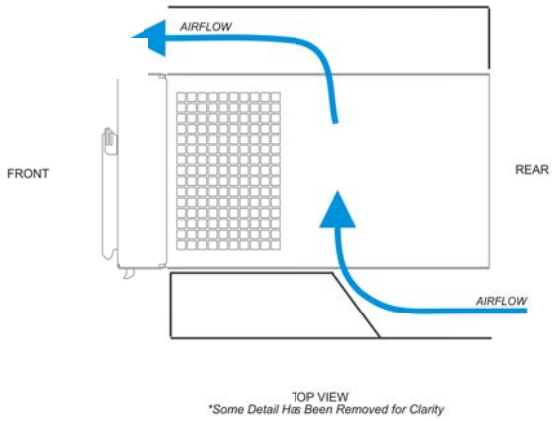
A.3.1 Flow Paths

The CMM can be placed into any SSI-compliant chassis, therefore the thermal solution (including heat sinks if any) must function in all airflow direction scenarios listed. Enabling the CMM thermal solution to function in these various air flow paths will provide system integrators with flexibility in developing overall air mover architectures and system layouts.

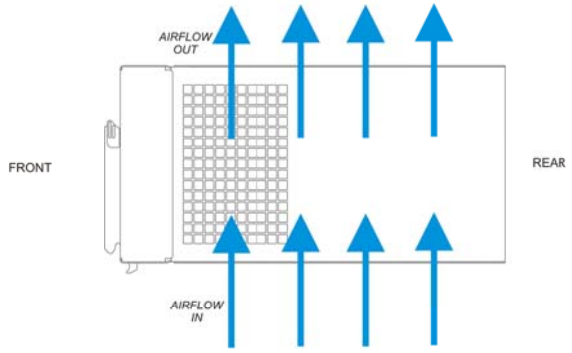
Airflow can be (see Figure A-6):

- Left to right.
- Right to left.
- Rear to top.
- Side to top.
- Rear to side(s).

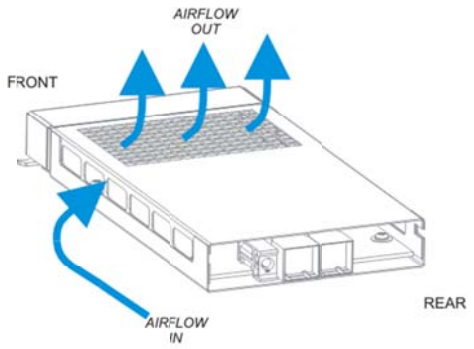
Figure A-6: Possible Airflow Paths



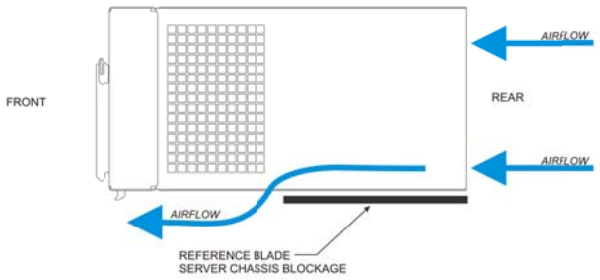
TOP VIEW
*Some Detail Has Been Removed for Clarity



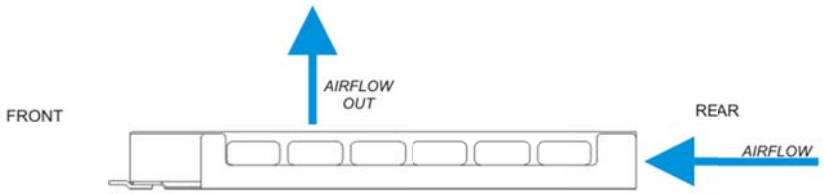
TOP VIEW
*Some Detail Has Been Removed for Clarity



*Some Detail Has Been Removed for Clarity



TOP VIEW
*Some Detail Has Been Removed for Clarity



SIDE VIEW
*Some Detail Has Been Removed for Clarity

A.3.2 Airflow and Impedance Requirements

A maximum flow rate of 10 CFM or lower is required to enable the integrator to cool the CMM with off the shelf airmovers, while meeting acoustic requirements. Final designs must operate thermally below the curves shown in Figure A-7 and Figure A-8.

Acoustic flow rates will be determined by system integrators, CMM's utilized, and end-user requirements.

The CMM manufacturer is required to provide validation information to system integrators. This could include, but not be limited to:

- Thermocouple locations.
- Recommended maximum temperatures of monitored devices.
- A Thermal Test Vehicle for pre-power on validation.
- A detailed thermal model.

See Figure A-9 for flow impedance verification.

Figure A-7: Module Flow rate requirements

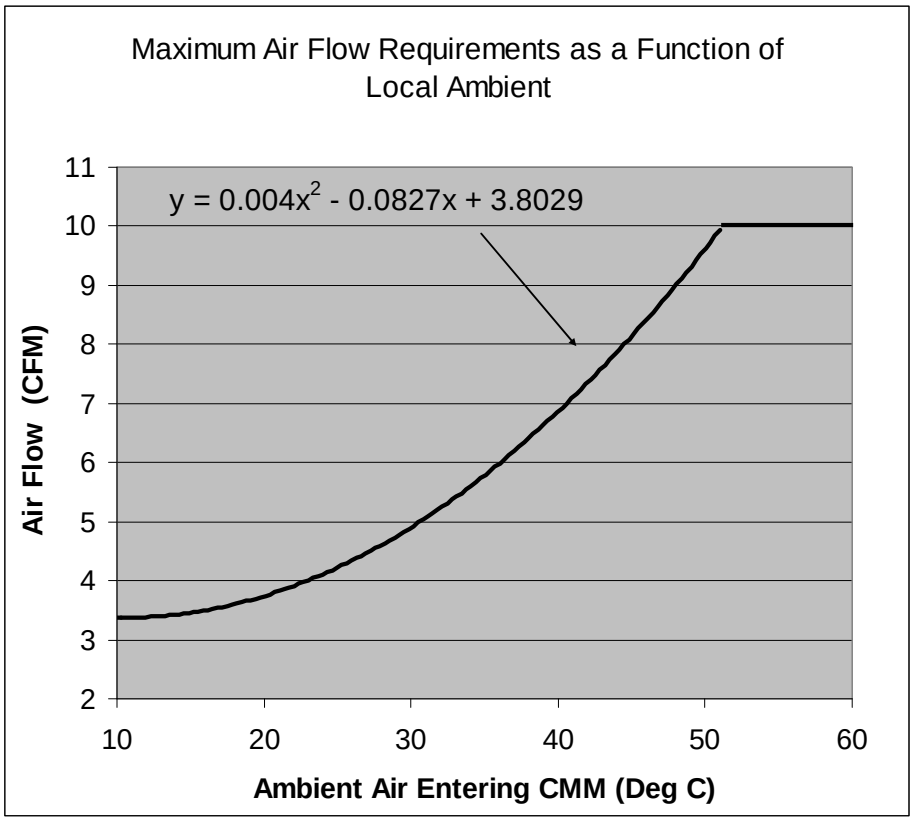
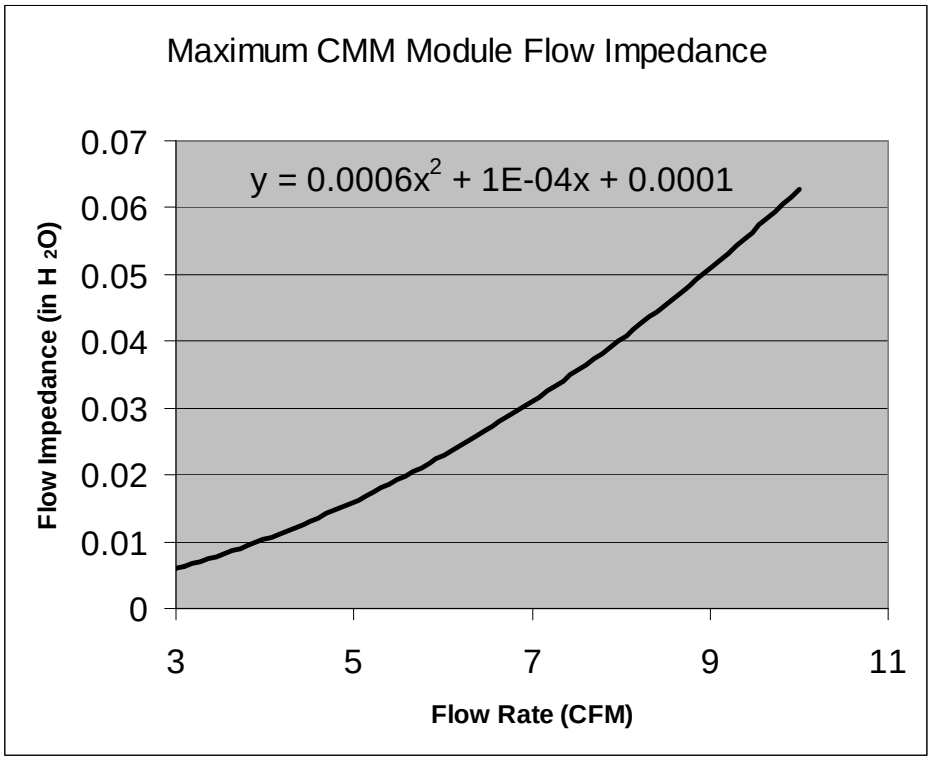


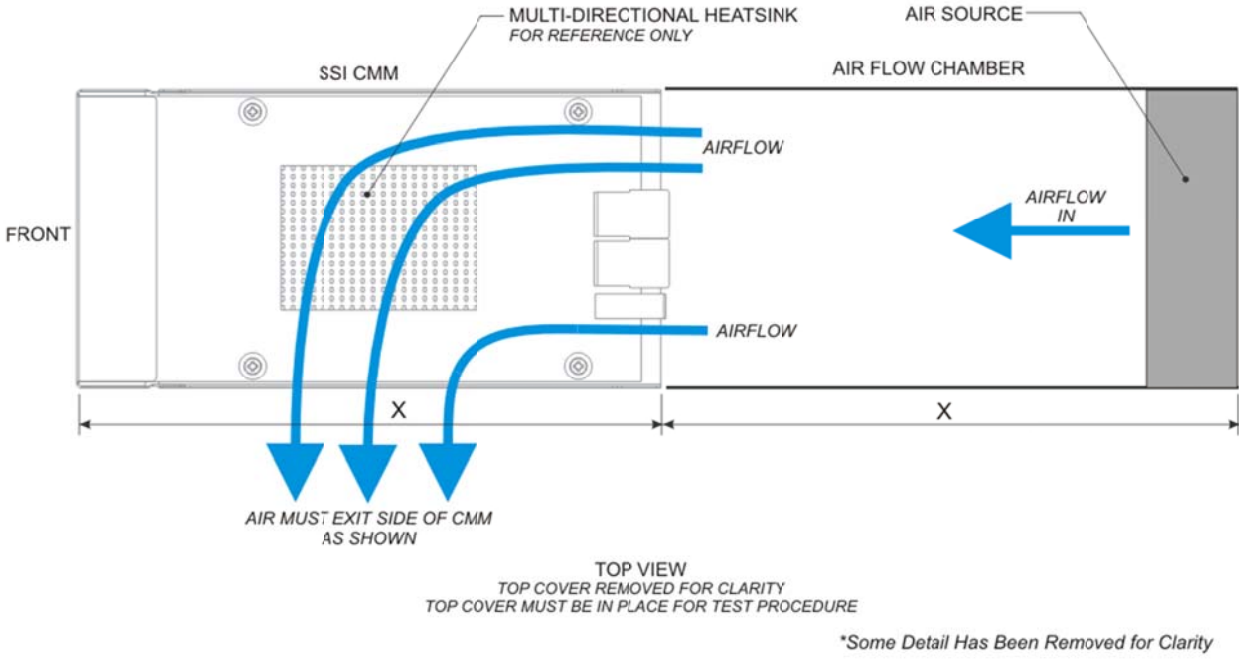
Figure A-8: Module Airflow Impedance Curve Requirements



Note: Final designs will vary, but thermal solutions must be enabled such that the CMM can function at or below the curves listed above. Integrators are responsible for ensuring proper flow delivery to the CMM.

The CMM module **shall not** exceed the impedance curve in Figure A-8. Verification that the CMM is in compliance can be tested via either detailed CFD thermal model or with a calibrated and properly instrumented wind tunnel. See Figure A-9 for details.

Figure A-9: Verifying Flow Impedance



CFD model set up

A.3.3 Mechanical Enclosure Venting Requirements

Figure A-10 describes the venting required to allow sufficient airflow through the CMM module. All defined venting is required such that all SSI-compliant air flow paths are supported. Chassis solutions, at the discretion of system integrators, may or may not leverage all required CMM enclosure venting to achieve proper cooling. Figure A-11 shows the dimensions for vents.

Figure A-10: Venting Requirements

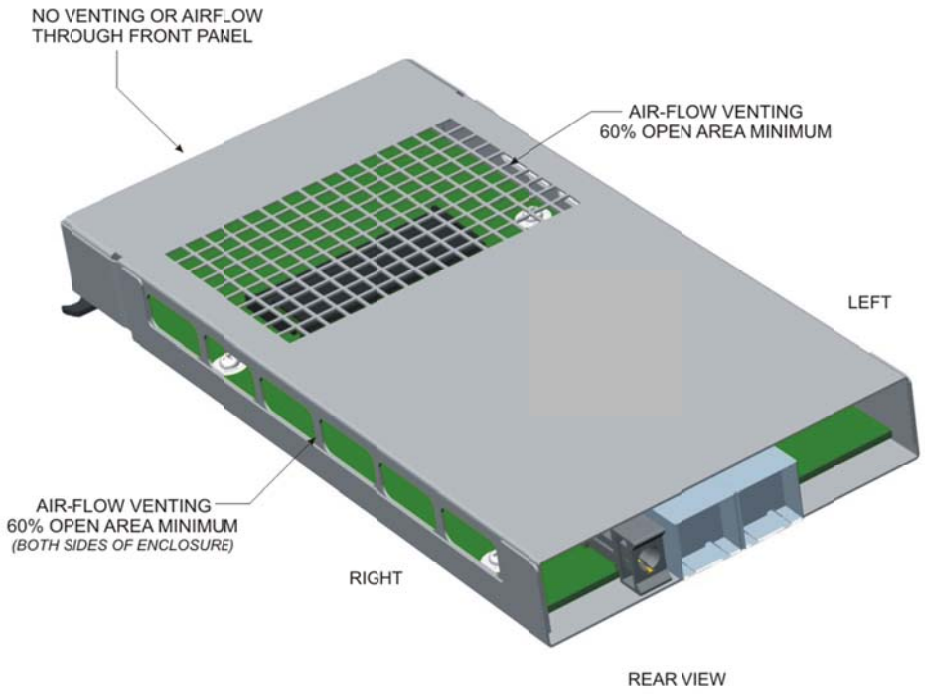
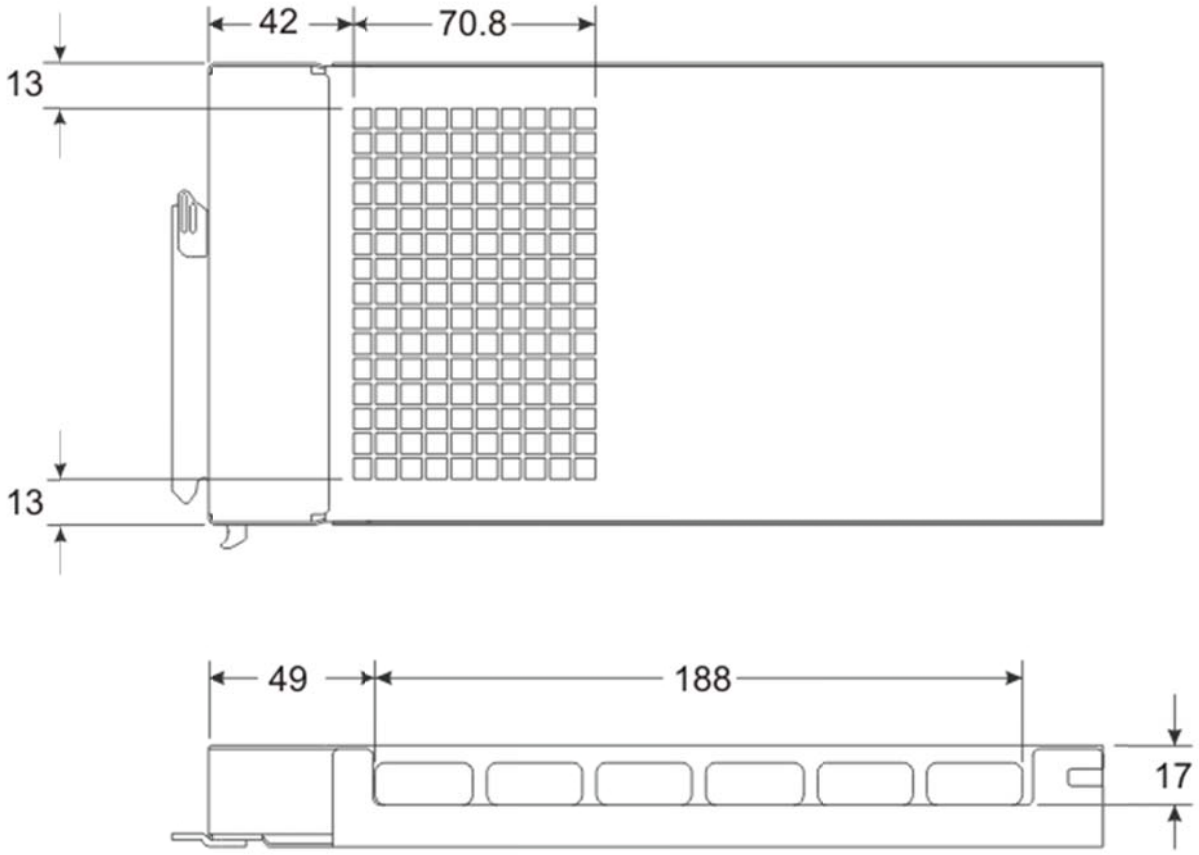


Figure A-11: Enclosure Mechanical Venting



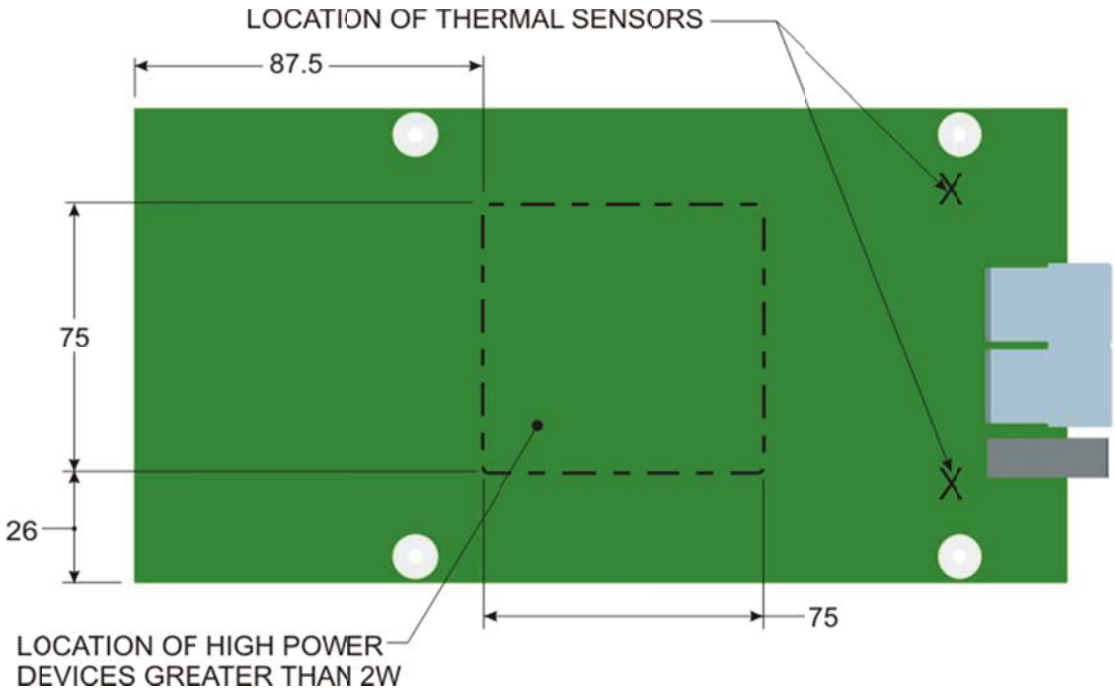
A.4 Component Placement and Sensor Requirements

A.4.1 Thermal Sensors

Local ambient temperature sensors are to be located approximately where shown in Figure A-12. Intent of these sensors is to measure incoming air temperatures (sometimes referred to as incoming local ambient) for any possible air flow schemes. Sensors should not be positioned close to any high power devices, which could skew the local ambient reading.

System designers and integrators will need to characterize these temperature sensors for their particular implementation.

Figure A-12: Location of Thermal Sensors:



A.4.2 High Power Devices

High powered devices, greater than 2 watts, are to be located in area indicated in Figure A-12. This is required in order to provide some uniformity from manufacturer to manufacturer, and to enable proper thermal operation from system to system.