BladeServer

Base Specification For I/O Expansion Cards

Document Version: 2.41
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Contents

Preface

1.1 Introduction

This document specifies the mechanical, electrical, logical and management aspects of the BladeServer I/O Expansion Cards. An I/O Expansion Card provides expansion I/O or functional capability for a Processor Blade. The I/O Expansion Card may or may not require a companion Switch Module to offer a complete range of function.

1.2 Document Control

All approved levels are 1.x and higher. The document is only available in PDF format.

1.3 Version Levels

Version	Date	Reason
0.5	1/29/2003	Preliminary specification (draft).
0.9	4/28/2003	Second draft
0.95	5/5/2003	Add VPD tables
0.99	6/18/2003	Added generic mechanical drawings
1.01	6/30/2003	Changed Telco temperature from 60 deg C to 67 deg C

1.4 Document Change History

Document change history will be maintained for versions 1.x and greater.

Version	Date	Reason
1.01	7/24/2003	First approved version
1.15	8/3/2004	Second approved version
1.21	11/22/2004	Added Small Form Factor (SFF) Daughter Card to Chapter 3, added shock and vibration as new Chapter 4, changed keepout area on bottom of standard daughter card, added thermal information to section 2.8
2.00	8/11/2005	Added High Speed Daughter Card
2.01	9/21/2005	Changed pin L25, PME_WAKE, to PCIE_WAKE Added thermal information
2.04	10/14/2005	Added mechanical drawings
2.05	11/18/2005	Changed Shock/Vib
2.06	1/18/2006	Changed mechanical drawings in Chapter 3
2.07	2/3/2006	Added Appendix A – Combo Form Factor
2.08	3/16/2006	Corrected Figure 2.8 (wrong pin numbering). Corrected figures 3.16, 3.17, 3.18, 3.22, 3.23, 3.24 (mislabeled “top” and “bottom”). Added tolerances to thickness on Figures 3.15 and 3.21.
2.10	2/07/2006	Replaced “Daughter Card” with “I/O Expansion Card”. Added CFFv and CFFh information to Chapters 1, 2, and 3. Removed Appendix A (Note that Appendix A referred to CFFE and CFFX which are now referred to as CFFh and CFFv respectively). Corrected Figure 3.18 and 3.24 titles (from component heights to 240VA). Updated connector part numbers in table for Figures 3.14 and 3.20. Added another connector supplier in Section 2.5. Re-Numbered Figures in Chapter 2.

		Incorporated updates as described in "UPDATE_Daughter_Card_5.15.2006.pdf ". Provided information for TBD's in Section 2.10. Provided max weight for CFFv and CFFh in Section 3.2. Marked holes on the LFF HSEC and HSEC that may be NPTH. Put connector part numbers from text throughout Section 2 into Tables below related text. Re-numbered Tables in Section 2 to accommodate added tables. Removed part numbers from Figures 3.3, 3.9, 3.14, & 3.20 and referenced connectors to appropriate table in Section 2, and mechanical items to mechanical design kits.
2.21	10/22/2007	Added Section 1.6. Updated Section 2.7 regarding AC blocking caps. Updated Section 2.11 to show correction to offset on the VPD read by the blade's BMC to A2. Updated Section 2.8.2 to reference the power plane tolerances per Section 2.8.1. Update to Maximum Temperature values for Table 2.3.1 (CFFv).
2.30	5/12/2008	Added Section 2.7. Updated Sections 2.8-13 regarding CIOv Expansion Cards. Updated Section 2.5 with HSEC connector pin list and PCI-E link assignment information. Updated Tables 1.1 and 2.6. Added Figures 2.6 and 3.37 – 3.40.
2.40	9/30/2008	Updated Sections 2.5.4, 2.5.5 HSEC connector pin list and PCI-E link assignment information.
2.41	2/06/2009	Updated signal names on tables 2.8, 2.9 and 2.16 through 2.19. Added section 2.15. Updated Section 2.12. Updated section 2.7.4 with text and fig. 2.13.

1.5 Change Frequency

This document will be updated to reflect changes and updates that are approved by the joint Intel/IBM Collaboration Architecture Review Board.

1.6 VPD Base Field for 'Base Specification Major and Minor Version'

Below is the information that must be initialized into the components VPD field described as 'Base Specification Major and Minor Version'. For an I/O Expansion Card component, this is the equivalent of the information as specified in the 'Document Version' on the title page of this specification. See 'Base Specification for VPD' for additional information.

Table 1.1 - Component VPD Field for 'Base Specification Major and Minor Version'

VPD Field Location	Hex Value in VPD	Displayed ASCII Value on MM Management Interfaces
Block1 (Dynamic Block Controller Area) byte offset: 01B2h	0229	'2.41.1'

2 I/O Expansion Card Design

2.1 Overview

The information in this document is not intended to provide sufficient details for final design of a product. Final design will require additional documents, including specific design practices and national and international standards that must be met. For example, knowledge of a product's intended geographical sales region will require meeting particular EMC and Safety requirements which cannot be called out in this document and which could affect the product design.

This document provides the interface and design specifications for I/O Expansion Cards that will attach to BladeServer Processor Blades. An I/O Expansion Card provides an expansion area for additional I/O functions or future processing expansion options. For example, two additional Ethernet Switch Modules can be installed in the rear of the BladeServer chassis in switch bays 3 and 4 and can be accessed from one or more Processor Blades via an I/O Expansion Card. Likewise, each processor can gain access to a Fibre Channel storage area network via an I/O Expansion Card and Switch Module combination. High Speed I/O Expansion Cards also attach to Processor Blades through a connector and can access High Speed Switch Modules located in any one of four High Speed Switch Module bays 7 through 10 located in the BladeServer High Speed (BSH) chassis.

I/O Expansion Cards defined in this specification include:

- I/O Expansion Card (EC)
- Small Form Factor I/O Expansion Card (SFF EC)
- High Speed I/O Expansion Card (HSEC)
- Large Form Factor High Speed I/O Expansion Card (LFF HSEC)
- Combo Form Factor V I/O Expansion Card (CFFv)
- Combo Form Factor H I/O Expansion Card (CFFh)
- CIOv I/O Expansion Card (CIOv)

The first four I/O Expansion cards listed above are mutually exclusive. Only one of these can be installed at any one time on a Processor Blade board. This means that, in a BladeServer High Speed chassis, a Single-Wide Blade can communicate with either the Legacy Switch Modules in Bays 3 and 4 or with the High Speed Switch Modules in Bays 7 through 10, but not both at the same time. However, the two Combo Form Factor I/O Expansion Cards can be used at the same time. These two form factors can be installed individually, just as the existing form factors. But, in addition, they can be installed simultaneously on any blade that supports both Legacy and High Speed form factor I/O Expansion Cards. The CFFv provides access to the Legacy Switch Modules 3 and 4, and the CFFh provides access to all of the High Speed Switch Modules.

There are numerous possibilities for function that can be deployed to an I/O Expansion Card and Switch Module. The interface and design specifications for Switch Modules and High Speed Switch Modules are contained in the Base Specification for Switch Module Subsystems.

2.2 I/O Expansion Card Placement on the Processor Blade

The following figures show the location of the various I/O Expansion Cards on a Processor Blade. It is recommended that the location of the EC, SFF EC, CFFv and CIOv is as shown. However, because these I/O Expansion Cards don't interface directly with the midplane of the BladeServer chassis, the

location is not fixed. The location of the HSEC, LFF HSEC, and the CFFh is fixed because they plug directly to the midplane.

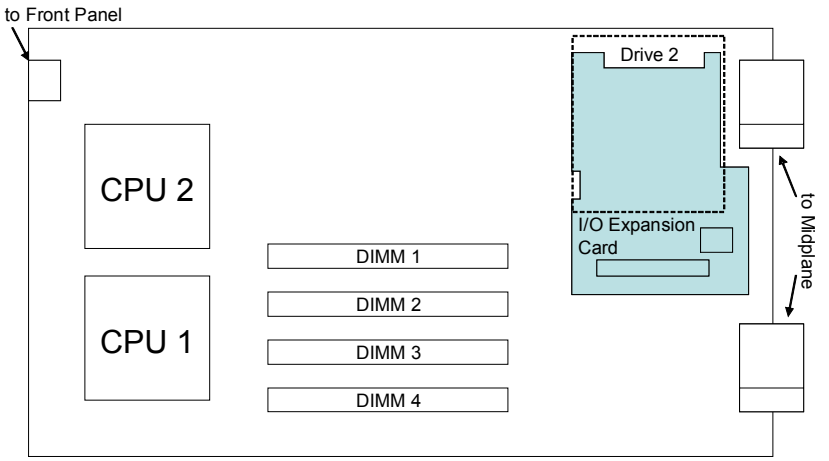


Figure 2.1. Example of a Processor Blade with I/O Expansion Card

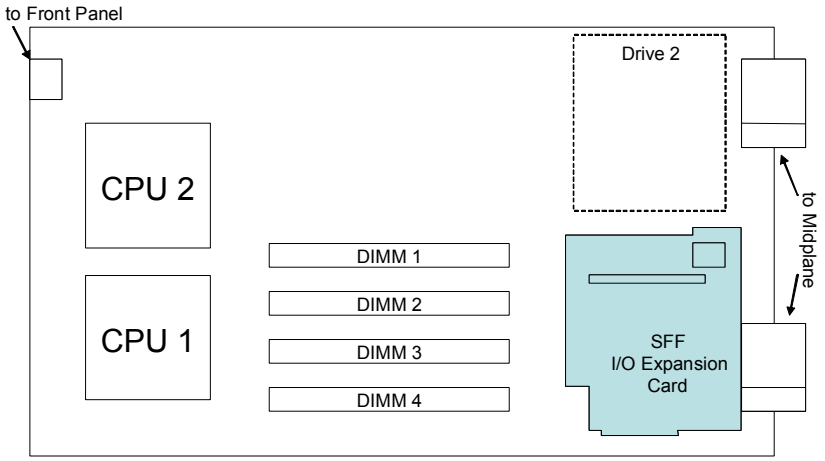


Figure 2.2. Example of a Processor Blade with SFF I/O Expansion Card

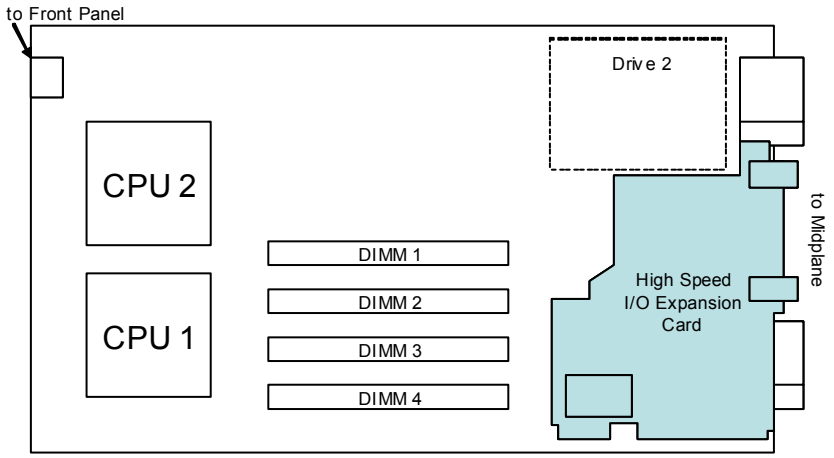


Figure 2.3. Example of a Processor Blade with a High Speed I/O Expansion Card

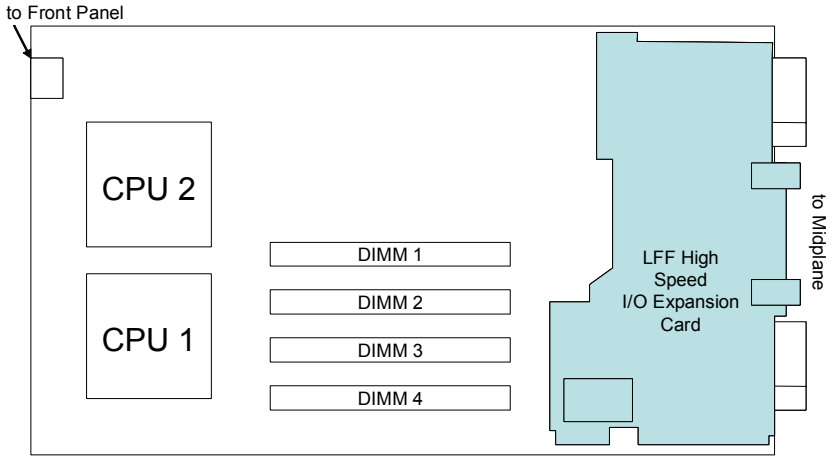


Figure 2.4. Example of a Processor Blade with a LFF High Speed I/O Expansion Card

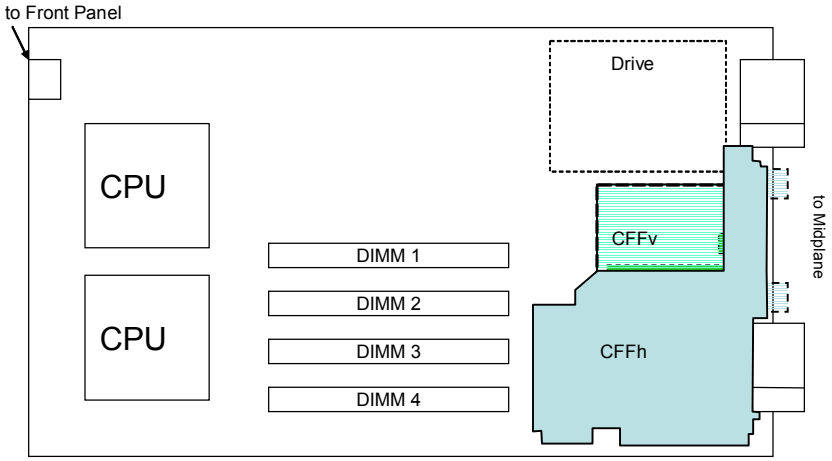


Figure 2.5. Example of a Processor Blade with a CFFv and CFFh

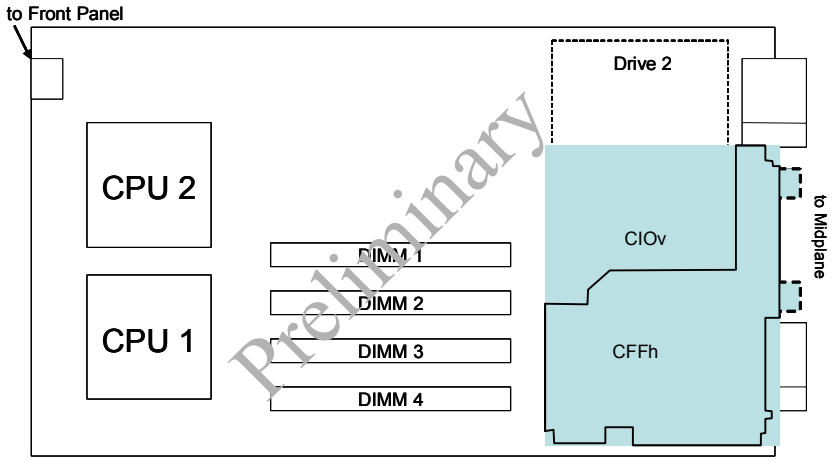


Figure 2.6. Example of Processor Blade with CFFh and CIOv

2.3 PCI-X Interface and Connector (EC, SFF EC, and CFFv I/O Expansion Cards)

The I/O Expansion Card supports a 64-bit PCI-X 1.0 electrical interface via a 200-pin (2x100) board-to-board stack connector (see Table 2.1). The mating connector on the blade may be found in Table 2.1. The card supports 3.3-volt signaling only. The PCI-X connector pin assignments are listed in Table 2.3. A bevel at one corner indicates pin 1. The other pins on the connector are numbered as shown in Table 2.3 (i.e. pin 101 is beside pin 1).

Table 2.1 – PCI-X Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
PCI Interface Connector (2x100)	Molex	500600-2079	--	--	Part of I/O Expansion Card
PCI Interface Connector (2x100)	Molex	500598-2079	--	--	Mating connector on Blade
Note: Refer to *BladeServer_Connectors_<yyyymmdd>.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/open_specs.html) for most up to date connector list.					

The I/O Expansion Card design should conform to the wiring and timing specifications in the PCI-X 1.0 specification, with the exception of the clock layout and PCIXCAP. Pull-up resistors (including IDSEL) are on the blade planar. The I/O Expansion Card does not require any pull-ups for the PCI-X signals.

IDSEL on Pin 20 of the PCI-X connector is for the first device. It is generated on the Blade using AD18 and a 2K series resistor on the blade. If a second device is present on the I/O expansion card, the IDSEL should be connected to AD19 through a 2K ohm series resistor on the I/O expansion card. Electrical validation of two devices on an I/O expansion card is the responsibility of the I/O expansion card designer.

2.3.1 PCI-X Clock Layout Requirements

The maximum PCI-X clock trace length is not the same as the standard of 2.5 inches. The blade application allows 3.5 inches from the surface of the blade, which must include the connector length of 0.59 inches. The minimum trace length is still the PCI-X minimum of 0.75 inches.

2.3.2 PCIXCAP

PCIXCAP is not implemented. See instead the PCIX_133 pin (pin 12) on the High Speed Mezzanine connector. PCIX_133 is used to differentiate between 100 MHz and 133 MHz bus speed. Pin 12 should be tied to ground on the I/O expansion card if the card supports 100 MHz PCI-X only. If the card supports 133 MHz, pin 12 should be NC. This means that all I/O expansion cards must operate in PCI-X mode and may not be PCI only.

2.3.3 Tables 2.2 and 2.3 contain additional information about pins on the 200-pin connector.

Table 2.2 - Additional Information for some Signals on the PCI-X Connector

Signal	Signal Type	Impedance/Coupling	Description
I2C_INT_N	OUTPUT OD AUX3_3V pull-up on system	55+/-10%	This is the I2C interrupt signal. This signal is used by those controllers that have the capability to send I2C alerts to a local BMC. Needed only if additional I2C devices other than VPD EEPROM present. The blade pulls this signal up to AUX3_3V via a 10K ohm resistor. See Note 1.
SCL	BIDIRECTIONAL AUX_3V pull-up on system	55+/-10%	100 KHz I^2C Serial Clock Lines. The BMC is the source of the clock, the I/O expansion card receives the clock. Pulled up to AUX3_3V via 2K-ohm resistor on blade.
SDA	BIDIRECTIONAL AUX3_3V pull-up on system	55+/-10%	100 KHz I^2C Serial Data Lines. The BMC is the source of the data lines, the I/O expansion card receives the data. Pulled up to AUX3_3V via 2K-ohm resistor on blade.
PRSNT1_N	OUTPUT	NA	This pin must be connected to PRSNT2_N. PRSNT1_N is pulled up to AUX3_3V via a 10K pull-up resistor on the blade. If there is no I/O expansion card installed, the BMC will detect this pin as high. If an I/O expansion card is installed, this pin will be pulled to ground.
PRSNT2_N	INPUT	NA	This pin must be connected to PRSNT1_N. PRSNT2_N is connected to ground on the blade.
SYS_PWR_GD	INPUT	NA	This input to the I/O expansion card indicates that all voltages are good.
PCIDIS_N	INPUT	NA	This signal should not be connected on the I/O expansion card.
ACTIVE_N	OUTPUT	NA	This signal is used to drive an LED via an open drain buffer located on the blade. It is pulled up to AUX3_3V via a 6.8K-ohm resistor. See Note 1.
REQ2_N	OUTPUT		This signal operates similar to REQ_N. This was provided to support an I/O expansion card that had two requests and grants. REQ_N must be used as the primary request. See Note 1.

GNT2_N	INPUT		This signal operates similar to GNT_N. This was provided to support an I/O expansion card that had two requests and grants. GNT_N must be used as the primary grant. See Note 1.

Note 1: This signal is pulled up on the blade and, if not used by the I/O expansion card, the pin should be left open.

Table 2.3 – I/O Expansion Card PCI-X Interface Connector Pin Assignments

PRSNT2_N	101	1	P12V	AD08	151	51	AD04
SYS_PWR_GD	102	2	PME_N	GND	152	52	GND
INTB_N	103	3	P5V	AD07	153	53	AD02
P5V	104	4	INTA_N	P3_3V	154	54	GND
REQ2_N	105	5	P5V	AD05	155	55	AD00
P5V	106	6	GNT2_N	GND	156	56	GND
CLK	107	7	P5V	AD03	157	57	REQ64_N
GND	108	8	RESET_N	GND	158	58	P3_3V
REQ_N	109	9	P5V	AD01	159	59	GND
P5V	110	10	GNT_N	P3_3V	160	60	CBE7_N
AD31	111	11	P5V	ACK64_N	161	61	GND
GND	112	12	AD30	GND	162	62	CBE5_N
AD29	113	13	P3_3V	PCIDIS_N	163	63	P3_3V
GND	114	14	AD28	GND	164	64	PAR64
AD27	115	15	GND	CBE6_N	165	65	GND
GND	116	16	AD26	GND	166	66	AD62
AD25	117	17	P3_3V	CBE4_N	167	67	GND
P3_3V	118	18	AD24	GND	168	68	AD60
CBE3_N	119	19	GND	AD63	169	69	GND
GND	120	20	IDSEL	GND	170	70	AD58
AD23	121	21	P3_3V	AD61	171	71	GND
GND	122	22	AD22	P3_3V	172	72	AD56
AD21	123	23	GND	AD59	173	73	GND
GND	124	24	AD20	GND	174	74	AD54
AD19	125	25	GND	AD57	175	75	P3_3V
P3_3V	126	26	AD18	GND	176	76	AD52
AD17	127	27	GND	AD55	177	77	GND
GND	128	28	AD16	GND	178	78	AD50
CBE2_N	129	29	P3_3V	AD53	179	79	GND
GND	130	30	FRAME_N	GND	180	80	AD48
IRDY_N	131	31	GND	AD51	181	81	GND
P3_3V	132	32	TRDY_N	GND	182	82	AD46
DEVSEL_N	133	33	GND	AD49	183	83	GND
GND	134	34	STOP_N	P3_3V	184	84	AD44
ACTIVE_N	135	35	P3_3V	AD47	185	85	GND
GND	136	36	GND	GND	186	86	AD42
PERR_N	137	37	PAR	AD45	187	87	GND
P3_3V	138	38	GND	GND	188	88	AD40
SERR_N	139	39	AD15	AD43	189	89	AUX3_3V
P3_3V	140	40	P3_3V	GND	190	90	AD38
CBE1_N	141	41	AD13	AD41	191	91	AUX3_3V
GND	142	42	GND	GND	192	92	AD36
AD14	143	43	AD11	AD39	193	93	AUX3_3V
GND	144	44	GND	P3_3V	194	94	AD34
AD12	145	45	AD09	AD37	195	95	GND
GND	146	46	GND	GND	196	96	AD32
AD10	147	47	CBE0_N	AD35	197	97	GND
GND	148	48	P3_3V	GND	198	98	SCL
M66EN	149	49	AD06	AD33	199	99	I2C_INT_N
GND	150	50	GND	PRSNT1_N	200	100	SDA

2.4 SERDES High Speed Differential Pairs and High Speed Mezzanine Connector (EC, SFF EC, and CFFv I/O Expansion Cards)

Four pairs of high-speed differential signals are connected to the Processor Blade by a high-speed mezzanine (HSM) connector (see Table 2.4). This connector has the potential for six pairs, but only four are used for high-speed signals. The mating connector on the blade may be found in Table 2.4. Figure 2.7 and Table 2.5 below indicate the pin assignments. Please refer to the "Base Specification for the Design of SERDES High-Speed Electrical Signaling."

Table 2.4 – High Speed Mezzanine Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
High Speed Connector	Molex	75003-2100	--	--	Part of I/O Expansion Card
High Speed Connector	Molex	75005-2100	--	--	Mating connector on Blade
Note: Refer to *BladeServer_Connectors_<yyyymmdd>.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/open_specs.html) for most up to date connector list.					

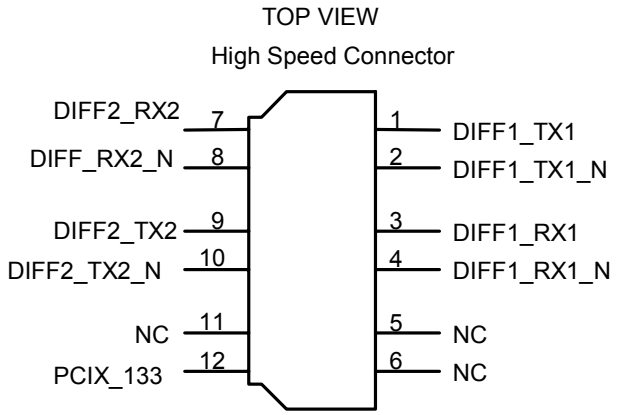


Figure 2.7. I/O expansion card differential pair connector

Table 2.5 –I/O Expansion Card Connector Pin Assignments High-speed Network Interface

Pin	Signal Name	Blade Midplane Connector	Pin	Signal Name	Blade Midplane Connector
1	DIFF1_TX1	TXP_2_CONN1	**7**	DIFF2_RX2	RXP_2_CONN2
2	DIFF1_TX1_N	TXN_2_CONN1	**8**	DIFF2_RX2_N	RXN_2_CONN2
3	DIFF1_RX1	RXP_2_CONN1	**9**	DIFF2_TX2	TXP_2_CONN2
4	DIFF1_RX1_N	RXN_2_CONN1	**10**	DIFF2_TX2_N	TXN_2_CONN2
5	NC	NC	**11**	NC	NC
6	NC	NC	**12**	PCIX_133	PCIX_133

Pin 12 should be tied to ground on the I/O expansion card if the card supports 100 MHz PCI-X only. If the card supports 133 MHz, pin 12 should be NC.

2.5 PCI-Express Interface and Connector (HSEC, LFF HSEC, CFFh I/O Expansion Cards)

The High Speed I/O Expansion Card supports a PCI Express (PCI-E) interface to the Blade via a 450-pin surface-mount BGA connector (see Table 2.6). The mating connector on the Blade may be found in Table 2.6. Figure 2.8 shows the stacking height of the PCI-E plug and receptacle.

Table 2.6 – PCI-E Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
PCI-Express Interface Connector, 200 signals, Receptacle	FCI	10069344-001	Tyco	1888922-5	Part of High Speed I/O Expansion Card
PCI-Express Interface Connector, 200 signals, Plug	FCI	10060910-001	Tyco	1-1888920-3	Mating connector on Blade
Note: Refer to *BladeServer_Connectors_<yyyymmdd>.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/open_specs.html) for most up to date connector list.					

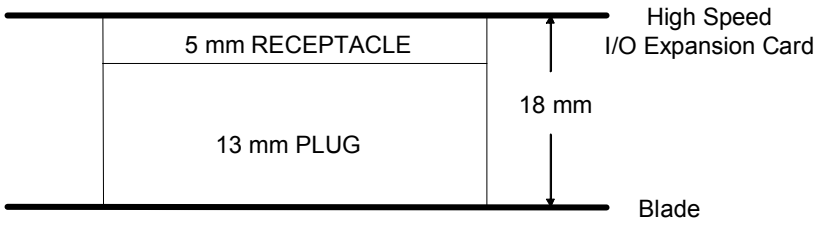


Figure 2.8. Stacking height of the PCI-E connectors

The signal names are assigned with respect to the Blade. In other words, the PCI-E signals that are outputs from the Blade will connect to the TX pins on the PCI-E HSEC connector.

2.5.1 PCI-E Specification Support

The HSEC will functionally comply with the PCI Express Base Specification Revision 1.0a maintained by the PCI SIG, with the exceptions of mechanical design and (potentially) power delivery. Due to the high-density packaging of BladeServer products, the PCI-E option family cannot fully comply with the PCI Express Card Electromechanical (CEM) Specification, particularly in the areas of form-factor and physical interconnect.

2.5.2 Polarity Inversion

The PCI-E specification requires all devices to support polarity inversion on their receivers. That is, the D^+ and D^- signals of each differential pair may be swapped during implementation if necessary. Each receiver is responsible for detecting an inversion during the training sequence and inverting the received signal if necessary. The HSEC must use PCI-E components that conform to the spec.

2.5.3 PCI-E Link Assignments

The PCI-E connector defines an aggregate total of 16 PCI-E lanes, broken into [up to] 4 logical links, as follows:

Link A0(x4): HSEC device (x4)
Link A1(x4): Bits [4:7] of x8 HSEC device
Link B0(x4): HSEC device (x4)
Link B1(x4): Bits [4:7] of x8 HSEC device, or second x4 HSEC device
Note: Links A and B are automatically configurable as full width links or multiple subset links (i.e.: Link B can be either one x8 link or two x4 links). When configured as a single x8 link:

Link B0 bits [0:3] correspond to Link B bits [0:3].
Link B1 bits [0:3] correspond to Link B bits [4:7]
Link A0 bits [0:3] correspond to Link A bits [0:3]
Link A1 bits [0:3] correspond to Link A bits [4:7]

HSEC designs should utilize the PCI-E lanes starting with B0 link and continue up to the A1 link. (i.e., a two chip HSEC design with a x8 link and x4 link requirement should implement the x8 device on the B0/B1 x8 links and the x4 device on the A0 link, while a single x16 device should have its lowest lane connected to B0[0] and the highest lane connected to A1[3]).

Blade PCI-E Bus B0 Signals require 26 Pins in the PCI-E connector.

- (4X) Transmit differential pairs (from Blade to PCI-E device)
- (4X) Receive differential pairs (from attached PCI-E device back to Blade)
- (1X) Link B0 Ref Clock differential pair (from Blade to PCI-E device)
- I2C interface for the PCI-E B Bus (Systems Management I2C bus to Blade)
- PCI-E B0 DIS pin: Disables devices on PCI-E Target on Bus B0
- PD PCIE B0 PRSNT pin: PCI-E target B0 presence pull-down (is pulled down on the Blade)
- PCIE B0 PRSNT pin: PCI-E target B0 presence indicator (this signal means that a device is attached onto the PCI-E B0 bus) This signal should be connected to the PD PCIE B0 PRSNT pin on the I/O expansion card

The disables are asserted by the Blade when it wants the device on that bus segment disabled.

PCI-E signal pin T1 (PD_PCIE_B0_PRSNT_N): This pin is pulled down on the Blade. Connect the T1 pin to A25 (PCIE_B0_PRSNT_N). This is used to perform a “continuity” function to ensure that the HSEC is seated in the connector.

PCI-E Bus B1 Signals require 20 Pins in the PCI-E connector.

- (4X) Transmit differential pairs (from Blade to PCI-E device)
- (4X) Receive differential pairs (from attached PCI-E device back to Blade)
- (1X) Link B1 Ref Clock differential pair (from Blade to PCI-E device)
- PCI-E B1 DIS pin: Disables devices on PCI-E Target on Bus B1

- PCIE B1 PRSNT pin: PCI-E target B1 presence indicator (this signal means that a device is attached onto the PCI-E B1 bus)

Pin B25 (PCIE_B1_PRSNT_N): PCI-E target B1 presence indicator.
If the only PCI-E device on the adapter is connected to link B0, this pin should remain high (leave open on the I/O expansion card). An adapter should drive this pin low if there is a device connected only to link B1. This could be an adapter with two PCI-E devices, one on link B0 and one on link B1, or an adapter with a just single device on link B1.

Blade PCI-E Bus A0 Signals require 26 Pins in the PCI-E connector.

- (4X) Transmit differential pairs (from Blade to PCI-E device)
- (4X) Receive differential pairs (from attached PCI-E device back to Blade)
- (1X) Link A0 Ref Clock differential pair (from Blade to PCI-E device)
- I2C interface for the PCI-E A0 Bus (Systems Management I2C bus to Blade)
- PCI-E A0 DIS pin: Disables devices on PCI-E Target on Bus A0
- PCIE A0 PRSNT pin: PCI-E target A0 presence indicator (this signal means that a device is attached onto the PCI-E A0 bus)

Blade PCI-E Bus A1 Signals require 26 Pins in the PCI-E connector.

- (4X) Transmit differential pairs (from Blade to PCI-E device)
- (4X) Receive differential pairs (from attached PCI-E device back to Blade)
- (1X) Link A1 Ref Clock differential pair (from Blade to PCI-E device)
- I2C interface for the PCI-E A1 Bus (Systems Management I2C bus to Blade)
- PCI-E A1 DIS pin: Disables devices on PCI-E Target on Bus A1
- PCIE A1 PRSNT pin: PCI-E target A1 presence indicator (this signal means that a device is attached onto the PCI-E A1 bus)

Pin T20 (PCIE_A1_PRSNT_N): PCI-E target A1 presence indicator.
If there is only a single x4 or x8 PCI-E device implemented on the A link, this pin should remain high (leave open on the I/O expansion card). An adapter should drive this pin low if there is a separate x4 device connected only to link A1. This could be an adapter with two PCI-E devices on the A link, one on link A0 and one on link A1, or an adapter with a just single device on link A1.

The two presence bits for each link, PCIE_A/B0_PRSNT_N and PCIE_A/B1_PRSNT_N, have slightly different meanings. If an HSEC consists of just one PCI-E device connected to link A/B0 (x4) or to links A/B0 and A/B1 (x8), it must have the PCIE_A/B0_PRSNT_N line asserted (pulled low on the I/O expansion card) to indicate to the blade that a PCI-E device is present. If an HSEC consists of two devices, or if the single device on the adapter is connected only to link A/B1 (x4), it must have both the PCIE_A/B0_PRSNT_N line and the PCIE_A/B1_PRSNT_N line asserted (pulled low on the I/O expansion card) to indicate to the blade that one or more PCI-E devices are present and that the PCI-E bus must be split into two x4 PCI-E links. The assertion of PCIE_A/B1_PRSNT_N informs the host system that the x8 link A/B needs to be split into 2 x4 links.

Table 2.7 - Example of Possible Expansion Card Designs and the Usage of the PCI-E Presence Bits
(Note: not all possible combinations are shown)

PCI-E Link Usage				PCI-E Presence Bits			
B0	B1	A0	A1	B0	B1	A0	A1
x4 device	No device	No device	No device	Yes	No	No	No
x4 device	x4 device	No device	No device	Yes	Yes	No	No
x8 device		No device	No device	Yes	No	No	No
x8 device		x4 device	No device	Yes	No	Yes	No

x8 device	X4 device	X4 device	Yes	No	Yes	Yes
x8 device	x8 device		Yes	No	Yes	No
X16 device			Yes	No	No	No

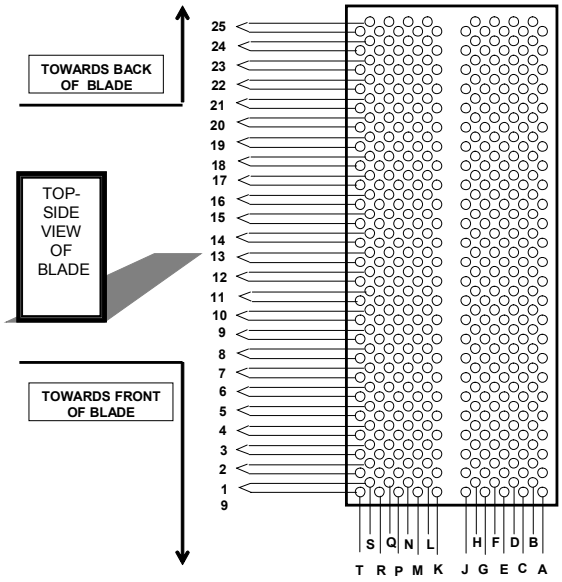


Figure 2.9. Pin numbering for the PCI-E connector

Figure 2.9 shows the connector pin numbering order for the PCI-E Connector that is located on the Blade. All pin numbers and signal names are referenced to the Blade. Figure 2.10 shows the orientation of the connector on the HSEC.

2.5.4 PCI-E Connector Pin List (Functional)

Note: Signal type is defined with respect to the HSEC option. Signals defined as OUT in these tables are driven by devices on the HSEC option, and signals defined as IN are driven by devices on the Blade.

Table 2.8 - PCI-E Connector Link A0 Signals

Signal Name	Pin #	Type	Description
PCIE_A_TX_0_P	Q16	IN	PCI-E bus A0 – bit 0 Transmit (True)
PCIE_A_TX_1_P	S16	IN	PCI-E bus A0 – bit 1 Transmit (True)
PCIE_A_TX_2_P	Q13	IN	PCI-E bus A0 – bit 2 Transmit (True)
PCIE_A_TX_3_P	S13	IN	PCI-E bus A0 – bit 3 Transmit (True)
PCIE_A_TX_0_N	Q17	IN	PCI-E bus A0 – bit 0 Transmit (Complement)
PCIE_A_TX_1_N	S17	IN	PCI-E bus A0 – bit 1 Transmit (Complement)
PCIE_A_TX_2_N	Q14	IN	PCI-E bus A0 – bit 2 Transmit (Complement)
PCIE_A_TX_3_N	S14	IN	PCI-E bus A0 – bit 3 Transmit (Complement)
PCIE_A_RX_0_P	L19	OUT	PCI-E bus A0 – bit 0 Receive (True)
PCIE_A_RX_1_P	N19	OUT	PCI-E bus A0 – bit 1 Receive (True)
PCIE_A_RX_2_P	L16	OUT	PCI-E bus A0 – bit 2 Receive (True)
PCIE_A_RX_3_P	N16	OUT	PCI-E bus A0 – bit 3 Receive (True)
PCIE_A_RX_0_N	L20	OUT	PCI-E bus A0 – bit 0 Receive (Complement)
PCIE_A_RX_1_N	N20	OUT	PCI-E bus A0 – bit 1 Receive (Complement)
PCIE_A_RX_2_N	L17	OUT	PCI-E bus A0 – bit 2 Receive (Complement)
PCIE_A_RX_3_N	N17	OUT	PCI-E bus A0 – bit 3 Receive (Complement)
CLK_PCIE_A0_P	L13	IN	Link A0 reference clock (True)
CLK_PCIE_A0_N	L14	IN	Link A0 reference clock (Complement)
PCIE_A0_DIS_N	N2	IN	Disable for PCI-E target on bus A0
<RESERVED>	Q2	IN	Reserved – do not connect
<RESERVED>	P2	IN	Reserved – do not connect
PCIE_A0_PRSNT_N	Q19	OUT	PCI-E target A0 presence indicator
I2C_A0_SCL	S2	BI	Systems management I2C bus to PCI-E Blade option on PCI-E bus A0
I2C_A0_SDA	T2	BI	
I2C_A0_INT_N	R1	OUT	
Total pins:	25		

Table 2.9 - PCI-E Connector Link A1 Signals

Signal Name	Pin #	Type	Description
PCIE_A_TX_4_P	Q10	IN	PCI-E bus A1 – bit 0 Transmit (True)
PCIE_A_TX_5_P	S10	IN	PCI-E bus A1 – bit 1 Transmit (True)
PCIE_A_TX_6_P	Q7	IN	PCI-E bus A1 – bit 2 Transmit (True)
PCIE_A_TX_7_P	S7	IN	PCI-E bus A1 – bit 3 Transmit (True)
PCIE_A_TX_4_N	Q11	IN	PCI-E bus A1 – bit 0 Transmit (Complement)
PCIE_A_TX_5_N	S11	IN	PCI-E bus A1 – bit 1 Transmit (Complement)
PCIE_A_TX_6_N	Q8	IN	PCI-E bus A1 – bit 2 Transmit (Complement)
PCIE_A_TX_7_N	S8	IN	PCI-E bus A1 – bit 3 Transmit (Complement)
PCIE_A_RX_4_P	N10	OUT	PCI-E bus A1 – bit 0 Receive (True)
PCIE_A_RX_5_P	F10	OUT	PCI-E bus A1 – bit 1 Receive (True)
PCIE_A_RX_6_P	N7	OUT	PCI-E bus A1 – bit 2 Receive (True)
PCIE_A_RX_7_P	N4	OUT	PCI-E bus A1 – bit 3 Receive (True)
PCIE_A_RX_4_N	N11	OUT	PCI-E bus A1 – bit 0 Receive (Complement)
PCIE_A_RX_5_N	F11	OUT	PCI-E bus A1 – bit 1 Receive (Complement)
PCIE_A_RX_6_N	N8	OUT	PCI-E bus A1 – bit 2 Receive (Complement)
PCIE_A_RX_7_N	N5	OUT	PCI-E bus A1 – bit 3 Receive (Complement)
CLK_PCIE_A1_P	N13	IN	Link A1 reference clock (True)
CLK_PCIE_A1_N	N14	IN	Link A1 reference clock (Complement)
PCIE_A1_DIS_N	N1	IN	Disable for PCI-E target on bus A1
<RESERVED>	S20	IN	Reserved – do not connect
<RESERVED>	R19	IN	Reserved – do not connect
PCIE_A1_PRSNT_N	T20	OUT	PCI-E target A1 presence indicator
I2C_A1_SCL	S1	BI	Systems management I2C bus to PCI-E Blade option on PCI-E bus A1
I2C_A1_SDA	G2	BI	
I2C_A1_INT_N	Q1	OUT	
Total pins:	25		

Table 2.10 - PCI-E Connector Link B0 Signals

Signal Name	Pin #	Type	Description
PCIE_B_TX_0_P	L4	IN	PCI-E bus B0 – bit 0 Transmit (True)
PCIE_B_TX_1_P	H13	IN	PCI-E bus B0 – bit 1 Transmit (True)
PCIE_B_TX_2_P	D13	IN	PCI-E bus B0 – bit 2 Transmit (True)
PCIE_B_TX_3_P	D10	IN	PCI-E bus B0 – bit 3 Transmit (True)
PCIE_B_TX_0_N	L5	IN	PCI-E bus B0 – bit 0 Transmit (Complement)
PCIE_B_TX_1_N	H14	IN	PCI-E bus B0 – bit 1 Transmit (Complement)
PCIE_B_TX_2_N	D14	IN	PCI-E bus B0 – bit 2 Transmit (Complement)
PCIE_B_TX_3_N	D11	IN	PCI-E bus B0 – bit 3 Transmit (Complement)
PCIE_B_RX_0_P	S4	OUT	PCI-E bus B0 – bit 0 Receive (True)
PCIE_B_RX_1_P	L7	OUT	PCI-E bus B0 – bit 1 Receive (True)
PCIE_B_RX_2_P	B13	OUT	PCI-E bus B0 – bit 2 Receive (True)
PCIE_B_RX_3_P	B10	OUT	PCI-E bus B0 – bit 3 Receive (True)
PCIE_B_RX_0_N	S5	OUT	PCI-E bus B0 – bit 0 Receive (Complement)
PCIE_B_RX_1_N	L8	OUT	PCI-E bus B0 – bit 1 Receive (Complement)
PCIE_B_RX_2_N	B14	OUT	PCI-E bus B0 – bit 2 Receive (Complement)
PCIE_B_RX_3_N	B11	OUT	PCI-E bus B0 – bit 3 Receive (Complement)
CLK_PCIE_B0_P	B4	IN	Link B0 reference clock (True)
CLK_PCIE_B0_N	B5	IN	Link B0 reference clock (Complement)
PCIE_B0_DIS_N	T19	IN	Disable for PCI-E target on bus B0. This is used to assert the chip's disable input or, in the absence of a disable pin, to hold the chip in reset by logically OR'ing it with the chip's reset input.
<RESERVED>	E25		Reserved – do not connect
<RESERVED>	D25		Reserved – do not connect
PD_PCIE_B0_PRSNT_N	T1	IN	PCI-E target B0 presence pull-down (pulled down on host system).
PCIE_B0_PRSNT_N	A25	OUT	PCI-E target B0 presence indicator
I2C_B_SCL	H25	BI	Systems management I2C bus to PCI-E Blade option on PCI-E bus B. Pull-ups are provided on the Blade.
I2C_B_SDA	H2	BI	
I2C_B_INT_N	R25	OUT	
Total pins:	26		

Table 2.11 - PCI-E Connector Link B1 Signals

Signal Name	Pin #	Type	Description
PCIE_B_TX_4_P	D4	IN	PCI-E bus B1 – bit 0 Transmit (True)
PCIE_B_TX_5_P	Q4	IN	PCI-E bus B1 – bit 1 Transmit (True)
PCIE_B_TX_6_P	H4	IN	PCI-E bus B1 – bit 2 Transmit (True)
PCIE_B_TX_7_P	H10	IN	PCI-E bus B1 – bit 3 Transmit (True)
PCIE_B_TX_4_N	D5	IN	PCI-E bus B1 – bit 0 Transmit (Complement)
PCIE_B_TX_5_N	Q5	IN	PCI-E bus B1 – bit 1 Transmit (Complement)
PCIE_B_TX_6_N	H5	IN	PCI-E bus B1 – bit 2 Transmit (Complement)
PCIE_B_TX_7_N	H11	IN	PCI-E bus B1 – bit 3 Transmit (Complement)
PCIE_B_RX_4_P	F4	OUT	PCI-E bus B1 – bit 0 Receive (True)
PCIE_B_RX_5_P	D7	OUT	PCI-E bus B1 – bit 1 Receive (True)
PCIE_B_RX_6_P	B7	OUT	PCI-E bus B1 – bit 2 Receive (True)
PCIE_B_RX_7_P	H7	OUT	PCI-E bus B1 – bit 3 Receive (True)
PCIE_B_RX_4_N	F5	OUT	PCI-E bus B1 – bit 0 Receive (Complement)
PCIE_B_RX_5_N	D8	OUT	PCI-E bus B1 – bit 1 Receive (Complement)
PCIE_B_RX_6_N	B8	OUT	PCI-E bus B1 – bit 2 Receive (Complement)
PCIE_B_RX_7_N	H8	OUT	PCI-E bus B1 – bit 3 Receive (Complement)
CLK_PCIE_B1_P	L10	IN	Link B1 reference clock (True)
CLK_PCIE_B1_N	L11	IN	Link B1 reference clock (Complement)
PCIE_B1_DIS_N	S19	IN	Disable for PCI-E target on bus B1. This is used to assert the chip's disable input or, in the absence of a disable pin, to hold the chip in reset by logically OR'ing it with the chip's reset input.
PCIE_B1_PRSNT_N	B25	OUT	PCI-E target B1 presence indicator
Total pins:	20		

Table 2.12 - PCI-E Connector Misc. Signals

Signal Name	Pin #	Type	Description
HOST_RST_OUT_N	C25	IN	Global Reset signal to PCI-E options.
<RESERVED>	P25		Reserved – do not connect
OPT_PCIE_WAKE	L25	OUT	PCI Express Wake indicator from PCI-E options
<RESERVED>	G1		Reserved – do not connect
PGOOD_HOST_AUX	N25	IN	Standby power-good indicator to PCI-E options
PGOOD_HOST_ALL	Q25	IN	Runtime power-good indicator to PCI-E options
<RESERVED>	T25		Reserved – do not connect
<RESERVED>	M25		Reserved – do not connect
<RESERVED>	S25		Reserved – do not connect
<RESERVED>	F7		Reserved – do not connect
OPT_ACTIVITY_N	P1	OUT	Activity indicator from PCI-E options. This signal is mandatory. It does not drive an LED directly.
<RESERVED>	M1		Reserved – do not connect
<RESERVED>	L1		Reserved – do not connect
<RESERVED>	Q20		Reserved – do not connect
<RESERVED>	R20		Reserved – do not connect
<RESERVED>	F8		Reserved – do not connect
Total pins:	16		

Table 2.13 - PCI-E Connector RMII Interface Pins

HSEC_ETH_RMII_TXD_0	H16	IN	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_TXD_1	H17	IN	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_RXD_0	F16	OUT	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_RXD_1	F17	OUT	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_DV	F13	OUT	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_TXEN	F14	IN	Used on ENET HSEC PCI-E Options
HSEC_ETH_RMII_50MHZ	H19	IN	Used on ENET HSEC PCI-E Options
Total pins:	7		

Note: the RMII Package ID for the HSEC card must be set to “0” for proper operation. If two devices are used on the HSEC, the ARB NCSI interface can be utilized locally on the expansion card. In this case, the first HSEC device should be set to “0” and the second HSEC device should be set to “2”.

All RMII signals must be wired to a maximum of 3.5 inches of trace length.

Table 2.14 - PCI-E Connector Reserved Signals

Signal Name	Pin #	Type	Description
<RESERVED>	B16		Reserved – do not connect
<RESERVED>	B17		Reserved – do not connect
<RESERVED>	B19		Reserved – do not connect
<RESERVED>	B20		Reserved – do not connect
<RESERVED>	D16		Reserved – do not connect
<RESERVED>	D17		Reserved – do not connect
<RESERVED>	D19		Reserved – do not connect
<RESERVED>	D20		Reserved – do not connect
<RESERVED>	F19		Reserved – do not connect
<RESERVED>	F20		Reserved – do not connect
<RESERVED>	F22		Reserved – do not connect
<RESERVED>	F23		Reserved – do not connect
<RESERVED>	H1		Reserved – do not connect
<RESERVED>	H20		Reserved – do not connect
<RESERVED>	H22		Reserved – do not connect
<RESERVED>	H23		Reserved – do not connect
<RESERVED>	L2		Reserved – do not connect
<RESERVED>	L22		Reserved – do not connect
<RESERVED>	L23		Reserved – do not connect
<RESERVED>	N22		Reserved – do not connect
<RESERVED>	N23		Reserved – do not connect
<RESERVED>	Q22		Reserved – do not connect
<RESERVED>	Q23		Reserved – do not connect
<RESERVED>	S22		Reserved – do not connect
<RESERVED>	S23		Reserved – do not connect
Total pins:	25		

Table 2.15 - PCI-E Connector Power and Ground Signals

Signal Name	Pin #	Count	Description
PWR_3_3VAUX	F25, G24, G25	3	+3.3V standby supply pins for HSEC power.
PWR_3_3V	A1, A2, B1, B2, C1, C2, D1, D2	8	+3.3V runtime supply pins for HSEC power.
PWR_12V	A22, A23, B22, B23, C22, C23, D22, D23	8	+12V runtime supply pins for bulk of HSEC power needs.
GND	A[3:21], A24	20	Ground / return pins
GND	B3, B6, B9, B12, B15, B18, B21, B24	8	
GND	C[3:21], C24	20	
GND	D3, D6, D9, D12, D15, D18, D21, D24	8	
GND	E[1:24]	24	
GND	F[1:3], F6, F9, F12, F15, F18, F21, F24	10	
GND	G[3:23]	21	
GND	H3, H6, H9, H12, H15, H18, H21, H24	8	
GND	J[1:25]	25	
GND	K[1:25]	25	
GND	L3, L6, L9, L12, L15, L18, L21, L24	8	
GND	M[2:24]	23	
GND	N3, N6, N9, N12, N15, N18, N21, N24	8	
GND	P[3:24]	22	
GND	Q3, Q6, Q9, Q12, Q15, Q18, Q21, Q24	8	
GND	R[2:18], R[21:24]	21	
GND	S3, S6, S9, S12, S15, S18, S21, S24	8	
GND	T[3:18], T[21:24]	20	
	Total pins:	306	

2.5.5 PCI-E Connector Pinout (Physical)

Note: Physical pinout table is based on the orientation of the connector looking at a Blade with the chassis midplane interfaces on the right. Pin A1 is located in the bottom-left corner of the connector when viewed in this orientation.

Table 2.16 - PCI-E Connector Pinout (1 of 4)

	1	2	3	4	5	6	7	
T	PCIE_B0_PRSNT_N	I2C_A0_SDA	GND	GND	GND	GND	GND	T
S	I2C_A1_SCL	I2C_A0_SCL	GND	PCIE_B_RX0_P	PCIE_B_RX0_N	GND	PCIE_A_TX_7_P	S
R	I2C_A0_INT_N	GND	GND	GND	GND	GND	GND	R
Q	I2C_A1_INT_N	Reserved	GND	PCIE_B_TX5_P	PCIE_B_TX5_N	GND	PCIE_A_TX_6_P	Q
P	OPT_ACTIVITY_N	Reserved	GND	GND	GND	GND	GND	P
N	PCIE_A1_DIS_N	PCIE_A0_DIS_N	GND	PCIE_A_RX_7_P	PCIE_A_RX_7_N	GND	PCIE_A_RX_6_P	N
M	Reserved	GND	GND	GND	GND	GND	GND	M
L	Reserved	Reserved	GND	PCIE_B_TX0_P	PCIE_B_TX0_N	GND	PCIE_B_RX1_P	L
K	GND	GND	GND	GND	GND	GND	GND	K
J	GND	GND	GND	GND	GND	GND	GND	J
H	Reserved	I2C_B_SDA	GND	PCIE_B_TX6_P	PCIE_B_TX6_N	GND	PCIE_B_RX7_P	H
G	Reserved	I2C_A1_SDA	GND	GND	GND	GND	GND	G
F	GND	GND	GND	PCIE_B_RX4_P	PCIE_B_RX4_N	GND	Reserved	F
E	GND	GND	GND	GND	GND	GND	GND	E
D	PWR_3_3V	PWR_3_3V	GND	PCIE_B_TX4_P	PCIE_B_TX4_N	GND	PCIE_B_RX5_P	D
C	PWR_3_3V	PWR_3_3V	GND	GND	GND	GND	GND	C
B	PWR_3_3V	PWR_3_3V	GND	CLK_PCIE_B0_P	CLK_PCIE_B0_N	GND	PCIE_B_RX6_P	B
A	PWR_3_3V	PWR_3_3V	GND	GND	GND	GND	GND	A
	1	2	3	4	5	6	7	

Table 2.17 - PCI-E Connector Pinout (2 of 4)

	8	9	10	11	12	13	
T	GND	GND	GND	GND	GND	GND	T
S	PCIE_A_TX_7_N	GND	PCIE_A_TX_5_P	PCIE_A_TX_5_N	GND	PCIE_A_TX_3_P	S
R	GND	GND	GND	GND	GND	GND	R
Q	PCIE_A_TX_6_N	GND	PCIE_A_TX_4_P	PCIE_A_TX_4_N	GND	PCIE_A_TX_2_P	Q
P	GND	GND	GND	GND	GND	GND	P
N	PCIE_A_RX_6_N	GND	PCIE_A_RX_4_P	PCIE_A_RX_4_N	GND	CLK_PCIE_A1_P	N
M	GND	GND	GND	GND	GND	GND	M
L	PCIE_B_RX1_N	GND	CLK_PCIE_B1_P	CLK_PCIE_B1_N	GND	CLK_PCIE_A0_P	L
K	GND	GND	GND	GND	GND	GND	K
J	GND	GND	GND	GND	GND	GND	J
H	PCIE_B_RX7_N	GND	PCIE_B_TX7_P	PCIE_B_TX7_N	GND	PCIE_B_TX1_P	H
G	GND	GND	GND	GND	GND	GND	G
F	Reserved	GND	PCIE_A_RX_5_P	PCIE_A_RX_5_N	GND	HSEC_ETH_RMII_DV_	F
E	GND	GND	GND	GND	GND	GND	E
D	PCIE_B_RX5_N	GND	PCIE_B_TX3_P	PCIE_B_TX3_N	GND	PCIE_B_TX2_P	D
C	GND	GND	GND	GND	GND	GND	C
B	PCIE_B_RX6_N	GND	PCIE_B_RX3_P	PCIE_B_RX3_N	GND	PCIE_B_RX2_P	B
A	GND	GND	GND	GND	GND	GND	A
	8	9	10	11	12	13	

Table 2.18 - PCI-E Connector Pinout (3 of 4)

	14	15	16	17	18	19	
T	GND	GND	GND	GND	GND	PCIE_B0_DIS_N	T
S	PCIE_A_TX_3_N	GND	PCIE_A_TX_1_P	PCIE_A_TX_1_N	GND	PCIE_B1_DIS_N	S
R	GND	GND	GND	GND	GND	<RESERVED>	R
Q	PCIE_A_TX_2_N	GND	PCIE_A_TX_0_P	PCIE_A_TX_0_N	GND	PCIE_A0_PRSNT_N	Q
P	GND	GND	GND	GND	GND	GND	P
N	CLK_PCIE_A1_N	GND	PCIE_A_RX_3_P	PCIE_A_RX_3_N	GND	PCIE_A_RX_1_P	N
M	GND	GND	GND	GND	GND	GND	M
L	CLK_PCIE_A0_N	GND	PCIE_A_RX_2_P	PCIE_A_RX_2_N	GND	PCIE_A_RX_0_P	L
K	GND	GND	GND	GND	GND	GND	K
J	GND	GND	GND	GND	GND	GND	J
H	PCIE_B_TX1_N	GND	HSEC_ETH_RMII_TXD_0	HSEC_ETH_RMII_TXD_1	GND	HSEC_ETH_RMII_50MHZ	H
G	GND	GND	GND	GND	GND	GND	G
F	HSEC_ETH_RMII_TXEN	GND	HSEC_ETH_RMII_RXD_0	HSEC_ETH_RMII_RXD_1	GND	Reserved	F
E	GND	GND	GND	GND	GND	GND	E
D	PCIE_B_TX2_N	GND	Reserved	Reserved	GND	Reserved	D
C	GND	GND	GND	GND	GND	GND	C
B	PCIE_B_RX2_N	GND	Reserved	Reserved	GND	Reserved	B
A	GND	GND	GND	GND	GND	GND	A
	14	15	16	17	18	19	

Table 2.19 - PCI-E Connector Pinout (4 of 4)

	20	21	22	23	24	25	
T	PCIE_A1_PRSNT_N	GND	GND	GND	GND	Reserved	T
S	<RESERVED>	GND	Reserved	Reserved	GND	Reserved	S
R	Reserved	GND	GND	GND	GND	I2C_B_INT_N	R
Q	Reserved	GND	Reserved	Reserved	GND	PGOOD_HOST_ALL	Q
P	GND	GND	GND	GND	GND	Reserved	P
N	PCIE_A_RX_1_N	GND	Reserved	Reserved	GND	PGOOD_HOST_AUX	N
M	GND	GND	GND	GND	GND	Reserved	M
L	PCIE_A_RX_0_N	GND	Reserved	Reserved	GND	OPT_PCIE_WAKE	L
K	GND	GND	GND	GND	GND	GND	K
J	GND	GND	GND	GND	GND	GND	J
H	Reserved	GND	Reserved	Reserved	GND	I2C_B_SCL	H
G	GND	GND	GND	GND	PWR_3_3VAUX	PWR_3_3VAUX	G
F	Reserved	GND	Reserved	Reserved	GND	PWR_3_3VAUX	F
E	GND	GND	GND	GND	GND	Reserved	E
D	Reserved	GND	PWR_12V	PWR_12V	GND	Reserved	D
C	GND	GND	PWR_12V	PWR_12V	GND	HOST_RST_OUT_N	C
B	Reserved	GND	PWR_12V	PWR_12V	GND	PCIE_B1_PRSNT_N	B
A	GND	GND	PWR_12V	PWR_12V	GND	PCIE_B0_PRSNT_N	A
	20	21	22	23	24	25	

2.6 High Speed I/O Expansion Card Midplane Connector (HSEC, LFF HSEC, CFFh I/O Expansion Cards)

The High Speed I/O Expansion Card connects directly to the Midplane through a 54 position right angle connector (see Table 2.20). The mating connector on the Midplane may be found in Table 2.20. Figure 2.10 shows the location of the connectors on a typical HSEC and Figure 2.11 shows the pin numbering for the connectors.

Table 2.20 – High Speed I/O Expansion Card / Midplane Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
Mezzanine Card Conn., 54 pos. Rt. Angle Header (Midplane Connector)	FCI	10058229-101LF	--	--	Part of High Speed I/O Expansion Card
Mating Conn. For Mezzanine Card Conn.	FCI	10039850-101LF	--	--	Mating connector on Midplane
Note: Refer to *BladeServer_Connectors_<yyyymmdd>.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/open_specs.html) for the most up-to-date connector list.					

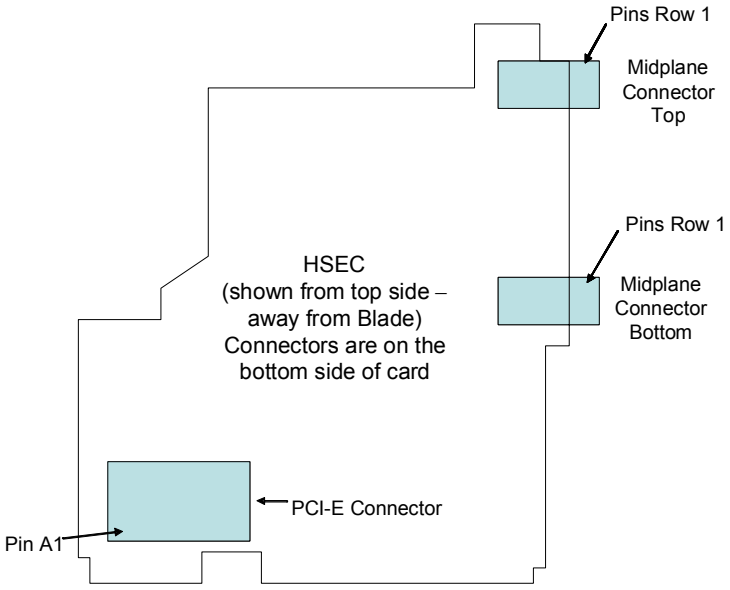


Figure 2.10. Location of connectors on a HSEC (typical)

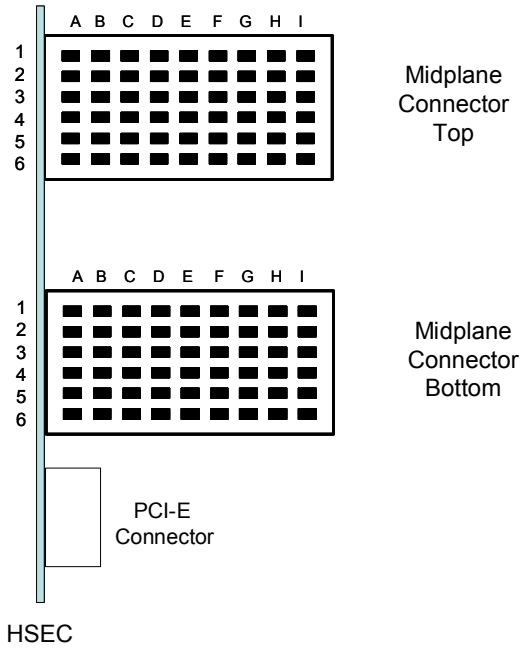


Figure 2.11. Pin numbering for the HSEC midplane connectors

2.6.1 HSEC Midplane Connector Pin Lists (Functional)

Table 2.21 - HSEC Midplane - Upper Connector

Signal Name	Pin #	Type	Description
TX_HSSM1_LN1_P	H4	OUT	to HSSM1, Lane 1 (True)
TX_HSSM1_LN2_P	G3	OUT	to HSSM1, Lane 2 (True)
TX_HSSM1_LN3_P	H2	OUT	to HSSM1, Lane 3 (True)
TX_HSSM1_LN4_P	G1	OUT	to HSSM1, Lane 4 (True)
TX_HSSM1_LN1_N	I4	OUT	to HSSM1, Lane 1 (Complement)
TX_HSSM1_LN2_N	H3	OUT	to HSSM1, Lane 2 (Complement)
TX_HSSM1_LN3_N	I2	OUT	to HSSM1, Lane 3 (Complement)
TX_HSSM1_LN4_N	H1	OUT	to HSSM1, Lane 4 (Complement)
RX_HSSM1_LN1_P	B6	IN	from HSSM1, Lane 1 (True)
RX_HSSM1_LN2_P	A5	IN	from HSSM1, Lane 2 (True)
RX_HSSM1_LN3_P	B4	IN	from HSSM1, Lane 3 (True)
RX_HSSM1_LN4_P	A3	IN	from HSSM1, Lane 4 (True)
RX_HSSM1_LN1_N	C6	IN	from HSSM1, Lane 1 (Complement)
RX_HSSM1_LN2_N	B5	IN	from HSSM1, Lane 2 (Complement)
RX_HSSM1_LN3_N	C4	IN	from HSSM1, Lane 3 (Complement)
RX_HSSM1_LN4_N	B3	IN	from HSSM1, Lane 4 (Complement)
TX_HSSM3_LN1_P	H6	OUT	to HSSM3, Lane 1 (True)

TX_HSSM3_LN2_P	G5	OUT	to HSSM3, Lane 2 (True)
TX_HSSM3_LN3_P	D3	OUT	to HSSM3, Lane 3 (True)
TX_HSSM3_LN4_P	E2	OUT	to HSSM3, Lane 4 (True)
TX_HSSM3_LN1_N	I6	OUT	to HSSM3, Lane 1 (Complement)
TX_HSSM3_LN2_N	H5	OUT	to HSSM3, Lane 2 (Complement)
TX_HSSM3_LN3_N	E3	OUT	to HSSM3, Lane 3 (Complement)
TX_HSSM3_LN4_N	F2	OUT	to HSSM3, Lane 4 (Complement)
RX_HSSM3_LN1_P	D5	IN	from HSSM3, Lane 1 (True)
RX_HSSM3_LN2_P	E4	IN	from HSSM3, Lane 2 (True)
RX_HSSM3_LN3_P	B2	IN	from HSSM3, Lane 3 (True)
RX_HSSM3_LN4_P	A1	IN	from HSSM3, Lane 4 (True)
RX_HSSM3_LN1_N	E5	IN	from HSSM3, Lane 1 (Complement)
RX_HSSM3_LN2_N	F4	IN	from HSSM3, Lane 2 (Complement)
RX_HSSM3_LN3_N	C2	IN	from HSSM3, Lane 3 (Complement)
RX_HSSM3_LN4_N	B1	IN	from HSSM3, Lane 4 (Complement)
Total pins: 32			

Table 2.22 - HSEC Midplane - Upper Connector – Misc. Signals

Signal Name	Pin #	Description
GND	A2, A4, A6	Ground/return pins
GND	C1, C3, C5	
GND	D2, D4, D6	
GND	F1, F3, F5	
GND	G2, G4, G6	
GND	I1, I3, I5	
KEY	D1, E1, E6, F6	NC: Do not connect on HSEC
Total pins: 22		

Note: Signal type is defined with respect to the HSEC. Signals defined as OUT in these tables are outputs from the HSEC.

Table 2.23 - HSEC Midplane - Lower Connector – Signals

Signal Name	Pin #	Type	Description
TX_HSSM2_LN1_P	H4	OUT	to HSSM2, Lane 1 (True)
TX_HSSM2_LN2_P	G3	OUT	to HSSM2, Lane 2 (True)
TX_HSSM2_LN3_P	H2	OUT	to HSSM2, Lane 3 (True)
TX_HSSM2_LN4_P	G1	OUT	to HSSM2, Lane 4 (True)
TX_HSSM2_LN1_N	I4	OUT	to HSSM2, Lane 1 (Complement)
TX_HSSM2_LN2_N	H3	OUT	to HSSM2, Lane 2 (Complement)
TX_HSSM2_LN3_N	I2	OUT	to HSSM2, Lane 3 (Complement)
TX_HSSM2_LN4_N	H1	OUT	to HSSM2, Lane 4 (Complement)
RX_HSSM2_LN1_P	B6	IN	from HSSM2, Lane 1 (True)
RX_HSSM2_LN2_P	A5	IN	from HSSM2, Lane 2 (True)
RX_HSSM2_LN3_P	B4	IN	from HSSM2, Lane 3 (True)
RX_HSSM2_LN4_P	A3	IN	from HSSM2, Lane 4 (True)
RX_HSSM2_LN1_N	C6	IN	from HSSM2, Lane 1 (Complement)
RX_HSSM2_LN2_N	B5	IN	from HSSM2, Lane 2 (Complement)
RX_HSSM2_LN3_N	C4	IN	from HSSM2, Lane 3 (Complement)
RX_HSSM2_LN4_N	B3	IN	from HSSM2, Lane 4 (Complement)
TX_HSSM4_LN1_P	H6	OUT	to HSSM4, Lane 1 (True)
TX_HSSM4_LN2_P	G5	OUT	to HSSM4, Lane 2 (True)
TX_HSSM4_LN3_P	D3	OUT	to HSSM4, Lane 3 (True)
TX_HSSM4_LN4_P	E2	OUT	to HSSM4, Lane 4 (True)
TX_HSSM4_LN1_N	I6	OUT	to HSSM4, Lane 1 (Complement)
TX_HSSM4_LN2_N	H5	OUT	to HSSM4, Lane 2 (Complement)
TX_HSSM4_LN3_N	E3	OUT	to HSSM4, Lane 3 (Complement)
TX_HSSM4_LN4_N	F2	OUT	to HSSM4, Lane 4 (Complement)
RX_HSSM4_LN1_P	D5	IN	from HSSM4, Lane 1 (True)
RX_HSSM4_LN2_P	E4	IN	from HSSM4, Lane 2 (True)
RX_HSSM4_LN3_P	B2	IN	from HSSM4, Lane 3 (True)
RX_HSSM4_LN4_P	A1	IN	from HSSM4, Lane 4 (True)
RX_HSSM4_LN1_N	E5	IN	from HSSM4, Lane 1 (Complement)
RX_HSSM4_LN2_N	F4	IN	from HSSM4, Lane 2 (Complement)
RX_HSSM4_LN3_N	C2	IN	from HSSM4, Lane 3 (Complement)
RX_HSSM4_LN4_N	B1	IN	from HSSM4, Lane 4 (Complement)
Total pins: 32			

Table 2.24 - HSEC Midplane - Lower Connector – Misc. Signals

Signal Name	Pin #	Description
GND	A2, A4, A6	Ground/return pins
GND	C1, C3, C5	
GND	D2, D4, D6	
GND	F1, F3, F5	
GND	G2, G4, G6	
GND	I1, I3, I5	
KEY	D1, E1, E6, F6	NC: Do not connect on HSEC
Total pins: 22		

2.6.2 Midplane Connector Pinouts (Physical)

Table 2.25 - Upper Connector Pinout

	1	2	3	4	5	6	
A	RX_HSSM3_LN4_P	GND	RX_HSSM1_LN4_P	GND	RX_HSSM1_LN2_P	GND	A
B	RX_HSSM3_LN4_N	RX_HSSM3_LN3_P	RX_HSSM1_LN4_N	RX_HSSM1_LN3_P	RX_HSSM1_LN2_N	RX_HSSM1_LN1_P	B
C	GND	RX_HSSM3_LN3_N	GND	RX_HSSM1_LN3_N	GND	RX_HSSM1_LN1_N	C
D	NC	GND	TX_HSSM3_LN3_P	GND	RX_HSSM3_LN1_P	GND	D
E	NC	TX_HSSM3_LN4_P	TX_HSSM3_LN3_N	RX_HSSM3_LN2_P	RX_HSSM3_LN1_N	NC	E
F	GND	TX_HSSM3_LN4_N	GND	RX_HSSM3_LN2_N	GND	NC	F
G	TX_HSSM1_LN4_P	GND	TX_HSSM1_LN2_P	GND	TX_HSSM3_LN2_P	GND	G
H	TX_HSSM1_LN4_N	TX_HSSM1_LN3_P	TX_HSSM1_LN2_N	TX_HSSM1_LN1_P	TX_HSSM3_LN2_N	TX_HSSM3_LN1_P	H
I	GND	TX_HSSM1_LN3_N	GND	TX_HSSM1_LN1_N	GND	TX_HSSM3_LN1_N	I
	1	2	3	4	5	6	

Table 2.26 - Lower Connector Pinout

	1	2	3	4	5	6	
A	RX_HSSM4_LN4_P	GND	RX_HSSM2_LN4_P	GND	RX_HSSM2_LN2_P	GND	A
B	RX_HSSM4_LN4_N	RX_HSSM4_LN3_P	RX_HSSM2_LN4_N	RX_HSSM2_LN3_P	RX_HSSM2_LN2_N	RX_HSSM2_LN1_P	B
C	GND	RX_HSSM4_LN3_N	GND	RX_HSSM2_LN3_N	GND	RX_HSSM2_LN1_N	C
D	NC	GND	TX_HSSM4_LN3_P	GND	RX_HSSM4_LN1_P	GND	D
E	NC	TX_HSSM4_LN4_P	TX_HSSM4_LN3_N	RX_HSSM4_LN2_P	RX_HSSM4_LN1_N	NC	E
F	GND	TX_HSSM4_LN4_N	GND	RX_HSSM4_LN2_N	GND	NC	F
G	TX_HSSM2_LN4_P	GND	TX_HSSM2_LN2_P	GND	TX_HSSM4_LN2_P	GND	G
H	TX_HSSM2_LN4_N	TX_HSSM2_LN3_P	TX_HSSM2_LN2_N	TX_HSSM2_LN1_P	TX_HSSM4_LN2_N	TX_HSSM4_LN1_P	H
I	GND	TX_HSSM2_LN3_N	GND	TX_HSSM2_LN1_N	GND	TX_HSSM4_LN1_N	I
	1	2	3	4	5	6	

2.7 PCI-Express & SERDES Interface and Connector (CIOv I/O Expansion Cards)

The CIOv High Speed I/O Expansion Card supports a PCI Express (PCI-E) and SERDES interface to the Blade via a 160-pin surface-mount connector (see Table 2.27). The mating connector on the Blade may be found in Table 2.6. Figure 2.12 shows the stacking height of the CIOv plug and receptacle.

Table 2.27 PCI-E Connectors

Connector Description	Source A		Source B		Note
	Vendor	Part Number	Vendor	Part Number	
PCI-Express & SERDES Interface Connector, 160 signals, Plug	Molex	46556-4145	N/A	N/A	Part of High Speed I/O Expansion Card
PCI-Express & SERDES Interface Connector, 160 signals, Receptacle	Molex	46557-4545	N/A	N/A	Mating connector on Blade
Note: Refer to *BladeServer_Connectors_<yyyymmdd>.pdf* located on the Blade Open Spec Support Center website (http://www-03.ibm.com/systems/bladecenter/open_specs.html) for most up to date connector list.					

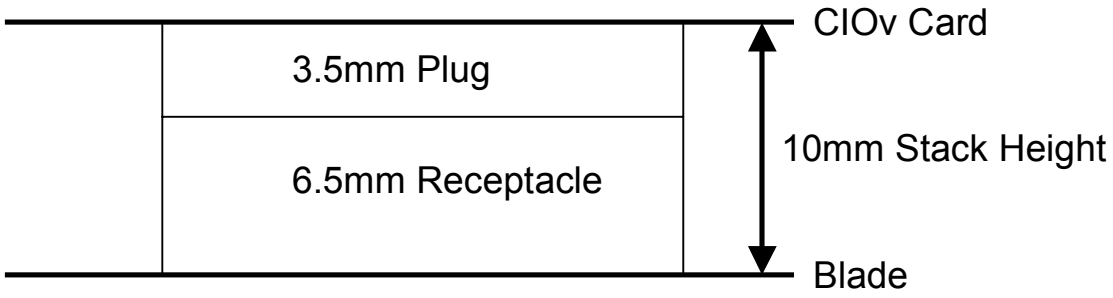


Figure 2.12. Stacking height of the CIOv plug and receptacle

2.7.1 PCI-E Specification Support

The CIOv will functionally comply with the PCI Express Base Specification Revision 2.0 maintained by the PCI SIG, with the exceptions of mechanical design and (potentially) power delivery. Due to the high-density packaging of BladeServer products, the PCI-E option family cannot fully comply with the PCI Express Card Electromechanical (CEM) Specification, particularly in the areas of form-factor and physical interconnect.

2.7.2 Polarity Inversion

The PCI-E specification requires all devices to support polarity inversion on their receivers. That is, the D^+ and D^- signals of each differential pair may be swapped during implementation if necessary. Each receiver is responsible for detecting an inversion during the training sequence and inverting the received signal if necessary. The CIOv must use PCI-E components that conform to the spec.

2.7.3 PCI-E Link Assignments

The PCI-E connector defines an aggregate total of 8 PCI-E lanes, supporting a single x8 device or a single x4 device

Link CIOv(x8): CIOv device (x8 or x4)

Blade PCI-E Bus CIOv Signals requires the following pins in the PCI-E connector.

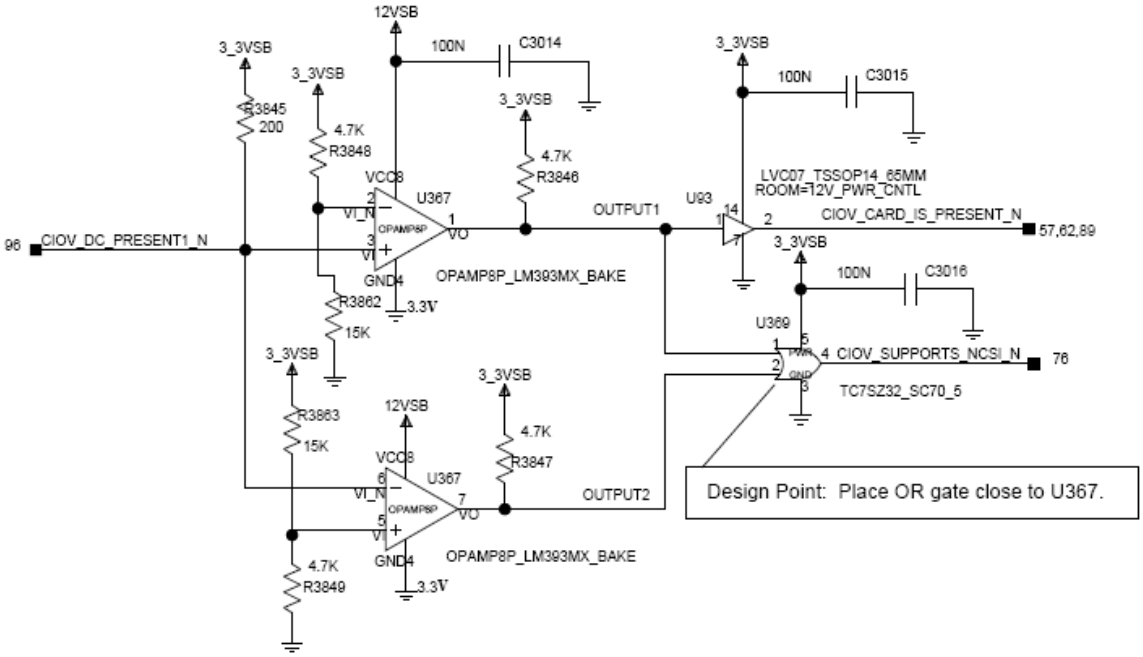
- (8X) Transmit differential pairs (from Blade to PCI-E device)
- (8X) Receive differential pairs (from attached PCI-E device back to Blade)
- (1X) Link Ref Clock differential pair (from Blade to PCI-E device)
- I2C interface for the PCI-E CIOv Bus (Systems Management I2C bus to Blade)
- PCIE_RESET_CIOv_N
- CIOv_DC_PRESENT2_N pin: PCI-E input presence pull-down (is pulled down on the Blade)
- CIOv_DC_PRESENT1_N pin: PCI-E target CIOv presence indicator (this signal means that a device is attached onto the PCI-E CIOv bus) This signal should be connected to the CIOv_DC_PRESENT2_N pin pin on the I/O expansion card

PCI-E signal pin 5 (CIOv_DC_PRESENT2_N): This pin is pulled down on the Blade by a 0ohm resistor. Ethernet CIOv expansion cards that utilize the RMII/NCSI interface, must connect pin 5

(CIOv_DC_PRESENT2_N) to pin 156 (CIOv_DC_PRESENT1_N) via a 200ohm resistor. All other expansion cards that do not use the RMII/NCSI interface must connect pin 5 (CIOv_DC_PRESENT2_N) to pin 156 (CIOv_DC_PRESENT1_N) via a 0hm resistor.

PCI-E signal pin 5 (CIOv_DC_PRESENT2_N): This pin is pulled down on the Blade by a 0ohm resistor. Ethernet CIOv expansion cards that utilize the RMII/NCSI interface, must connect pin 5 (CIOv_DC_PRESENT2_N) to pin 156 (CIOv_DC_PRESENT1_N) via a 200ohm resistor. All other expansion cards that do not use the RMII/NCSI interface must connect pin 5 (CIOv_DC_PRESENT2_N) to pin 156 (CIOv_DC_PRESENT1_N) via a 0hm resistor.

BladeServer designers must provide a comparator circuit to detect whether a 0ohm or 200ohm resistor has been implemented on the CIOv expansion card. The BladeServer must detect the voltage level on the CIOv_DC_PRESENT1_N signal from the CIOv expansion card and use the result to enable/disable the RMII/NCSI interface. If the voltage level is one half of 3.3VSB then the CIOv expansion card supports NCSI functionality. If the voltage level is ground then the CIOv expansion card does not support NCSI functionality. An example reference circuit for the BladeServer is provided below.



OUTPUT1	OUTPUT2	LOGIC DECODE
0	0	CIOV DC PRESENT & NCSI SUPPORTED
0	1	CIOV CARD PRESENT & NCSI NOT SUPPORTED
1	0	CARD NOT INSTALLED
1	1	IMPOSSIBLE STATE

Figure 2.13. Stacking height of the CIOv plug and receptacle

2.7.4 CIOv Connector Pin List

Note: Signal type is defined with respect to the CIOv option. Signals defined as OUT in these tables are driven by devices on the CIOv option, and signals defined as IN are driven by devices on the Blade.

Table 2.28 - CIOv Signals

Signal Name	Pin #	Type	Description
PCIE_CIOv _TX_0_P	144	IN	PCI-E bit 0 Transmit (True)
PCIE_CIOv _TX_1_P	145	IN	PCI-E bit 1 Transmit (True)
PCIE_CIOv _TX_2_P	133	IN	PCI-E bit 2 Transmit (True)
PCIE_CIOv _TX_3_P	128	IN	PCI-E bit 3 Transmit (True)
PCIE_CIOv _TX_0_N	140	IN	PCI-E bit 0 Transmit (Complement)
PCIE_CIOv _TX_1_N	149	IN	PCI-E bit 1 Transmit (Complement)
PCIE_CIOv _TX_2_N	129	IN	PCI-E bit 2 Transmit (Complement)
PCIE_CIOv _TX_3_N	124	IN	PCI-E bit 3 Transmit (Complement)
PCIE_CIOv _TX_4_P	117	IN	PCI-E bit 4 Transmit (True)
PCIE_CIOv _TX_5_P	108	IN	PCI-E bit 5 Transmit (True)
PCIE_CIOv _TX_6_P	101	IN	PCI-E bit 6 Transmit (True)
PCIE_CIOv _TX_7_P	96	IN	PCI-E bit 7 Transmit (True)
PCIE_CIOv _TX_4_N	113	IN	PCI-E bit 4 Transmit (Complement)
PCIE_CIOv _TX_5_N	112	IN	PCI-E bit 5 Transmit (Complement)
PCIE_CIOv _TX_6_N	97	IN	PCI-E bit 6 Transmit (Complement)
PCIE_CIOv _TX_7_N	92	IN	PCI-E bit 7 Transmit (Complement)
PCIE_CIOv _RX_0_P	44	OUT	PCI-E bit 0 Receive (True)
PCIE_CIOv _RX_1_P	53	OUT	PCI-E bit 1 Receive (True)
PCIE_CIOv _RX_2_P	80	OUT	PCI-E bit 2 Receive (True)
PCIE_CIOv _RX_3_P	28	OUT	PCI-E bit 3 Receive (True)
PCIE_CIOv _RX_0_N	48	OUT	PCI-E bit 0 Receive (Complement)
PCIE_CIOv _RX_1_N	49	OUT	PCI-E bit 1 Receive (Complement)
PCIE_CIOv _RX_2_N	76	OUT	PCI-E bit 2 Receive (Complement)
PCIE_CIOv _RX_3_N	32	OUT	PCI-E bit 3 Receive (Complement)
PCIE_CIOv _RX_4_P	69	OUT	PCI-E bit 4 Receive (True)
PCIE_CIOv _RX_5_P	85	OUT	PCI-E bit 5 Receive (True)
PCIE_CIOv _RX_6_P	60	OUT	PCI-E bit 6 Receive (True)
PCIE_CIOv _RX_7_P	33	OUT	PCI-E bit 7 Receive (True)
PCIE_CIOv _RX_4_N	65	OUT	PCI-E bit 4 Receive (Complement)
PCIE_CIOv _RX_5_N	81	OUT	PCI-E bit 5 Receive (Complement)
PCIE_CIOv _RX_6_N	64	OUT	PCI-E bit 6 Receive (Complement)
PCIE_CIOv _RX_7_N	37	OUT	PCI-E bit 7 Receive (Complement)

PCIE_CIOv _PECLK_P	99	IN	PCI-E reference clock (True)
PCIE_CIOv _PECLK_N	103	IN	PCI-E reference clock (Complement)
DIFF_CIOv_TX_1_P	90	OUT	SerDes Transmit to I/O BAY 3 (True)
DIFF_CIOv_TX_1_N	94	OUT	SerDes Transmit to I/O BAY 3 (Complement)
DIFF_CIOv_RX_1_P	74	IN	SerDes Receive from I/O BAY 3 (True)
DIFF_CIOv_RX_1_N	78	IN	SerDes Receive from I/O BAY 3 (Complement)
DIFF_CIOv_TX_2_P	71	OUT	SerDes Transmit to I/O BAY 4 (True)
DIFF_CIOv_TX_2_N	67	OUT	SerDes Transmit to I/O BAY 4 (Complement)
DIFF_CIOv_RX_2_P	87	IN	SerDes Receive from I/O BAY 4 (True)
DIFF_CIOv_RX_2_N	83	IN	SerDes Receive from I/O BAY 4 (Complement)
ETH_RMII_TXD_0	115	IN	Used on ENET CIOv PCI-E Options
ETH_RMII_TXD_1	119	IN	Used on ENET CIOv PCI-E Options
ETH_RMII_RXD_0	142	OUT	Used on ENET CIOv PCI-E Options
ETH_RMII_RXD_1	138	OUT	Used on ENET CIOv PCI-E Options
ETH_RMII_DV	135	OUT	Used on ENET CIOv PCI-E Options
ETH_RMII_TXEN	154	IN	Used on ENET CIOv PCI-E Options
ETH_RMII_50MHZ	131	IN	Used on ENET CIOv PCI-E Options
ETH_NCSI_ARBIN	126	OUT	Note: All non-ENET CIOv options must directly connect ETH_NCSI_ARBIN to ETH_NCSI_ARBOUT on the daughter card.
ETH_NCSI_ARBOUT	122	IN	Note: All non-ENET CIOv options must directly connect ETH_NCSI_ARBIN to ETH_NCSI_ARBOUT on the daughter card.
PCIE_RESET_CIOv_N	16	IN	PCI-E Reset
POWERGOOD_CIOv	12	IN	Power good signal from blade
CIOv_WAKE_N	7	OUT	Wake on LAN output from PCI-E Option
CIOv_DC_ACTIVITY_N	155	OUT	Activity output from PCI-E Option
CIOv_DC_PRESENT1_N	156	OUT	Connect to CIOv_DC_PRESENT2_N on PCI-E Option
CIOv_DC_PRESENT2_N	5	IN	GND Input from Blade
CIOv_I2C_SCL	151	BI	Systems management I2C bus to PCI-E Blade option
CIOv_I2C_SDA	147	BI	
CIOv_I2C_INT_N	152	OUT	
Total pins:	60		

Table 2.29 - CIOv Connector RESERVED, Power and Ground Signals

Signal Name	Pin #	Count	Description
3.3VSB	157	1	+3.3V standby supply pins for CIOv power.
3.3v	1, 2, 158, 159	4	+3.3V runtime supply pins for CIOv power.
5V	3, 4, 160	3	+5V runtime supply pins for CIOv power.
GND	9, 11, 15, 18, 22, 24, 25, 27, 29, 31, 34, 36, 38, 40, 41, 43, 45, 47, 50, 52, 54, 56, 57, 59, 61, 63, 66, 68, 70, 72, 73, 75, 77, 79, 82, 84, 86, 88, 89, 91, 93, 95, 98, 100, 102, 104, 105, 107, 109, 111, 114, 116, 118, 120, 121, 123, 125, 127, 130, 132, 134, 136, 137, 139, 141, 143, 146, 148, 150, 153	70	Ground / return pins
RESERVED	6, 8, 10, 13, 14, 17, 19, 20, 21, 23, 26, 30, 35, 39, 42, 46, 51, 55, 58, 62,106, 110	22	
	Total pins:	100	

2.7.5 RMII/NCSI Usage

Ethernet CIOv cards should connect the RMII interface and arbitration bus for proper blade support. For ALL CIOv expansion cards that will not use the RMII interface, pins 122 ETH_NCSI_ARBOUT and 126 ETH_NCSI_ARBIN must be connected together on the expansion card.

The RMII Package ID for the CIOv card must be set to “2” for proper operation.

All RMII signals must be wired to a maximum of 2.5” of trace length.

2.8 I/O Expansion Card Electrical Guidelines (HSEC, LFF HSEC, CFFh I/O Expansion Cards)

2.8.1 High Speed I/O Expansion Card Electrical Guidelines (HSEC, LFF HSEC, CFFh Expansion Cards)

. The wiring on the HSDC SERDES pairs must have DC blocking caps on both the TX and RX paths. An AC coupling capacitor in the range of 75-200 nF must be used on the transmitter side of each PCI-E signals and follow SERDES specification for placement and routing of capacitor. All High speed lines connected to Midplane require DC blocking capacitors on transmit and receive lines. DC blocking requires a broad range of low loss, resonant free, frequency coverage. The upper limit of bandwidth over which insertion loss meets specification is determined by the location of parallel resonances. For maximum resonant-free bandwidth, custom broadband blocks such as the DEL C06BLBB2X5UX family components are recommended.

The wiring on the HSEC for the PCI-E connections should target a differential impedance of 85Ω ± 10%. The wiring on the HSDC for SERDES connections should target a differential impedance of 100Ω ± 10%. Since most or all of the wiring in the BladeServer printed circuit boards is pseudo-differential (complementary single-ended transmission lines referencing a common plane), the single-ended impedance of the individual conductors should be taken into account when developing a printed circuit board cross-section.

Since the ground planes are the only reference planes that are guaranteed to be common across all printed circuit boards and connectors within the chassis, all high-speed wiring should reference only ground planes.

2.8.2 I/O Expansion Card Electrical Guidelines (CIOv)

The wiring on the CIOv SERDES pairs must have DC blocking caps on both the TX and RX paths. The CIOv PCI-E bus requires DC blocking caps on the TX signals originating from the expansion card. No caps are required on the PCIe clock signals. The recommended values for the capacitors are 0.1µF for the PCI-E signals, and 0.01µF for the Midplane connections.

The wiring on the CIOv for the PCI-E connections should target a differential impedance of 85Ω ± 10%. The wiring on the CIOv for the SERDES connections should target a differential impedance of 100Ω ± 10%. Since most or all of the wiring in the BladeServer printed circuit boards is pseudo-differential (complementary single-ended transmission lines referencing a common plane), the single-ended impedance of the individual conductors should be taken into account when developing a printed circuit board cross-section.

Since the ground planes are the only reference planes that are guaranteed to be common across all printed circuit boards and connectors within the chassis, all high-speed wiring should reference only ground planes.

2.9 I/O Expansion Card Power

2.9.1 I/O Expansion Card Power (EC, SFF EC, and CFFv I/O Expansion Cards)

The maximum power budget for the EC, SFF EC, and CFFv is 10 Watts/card (Although the numbers in Table 2.30 add up to more than 10 W, the power usage is limited to 10W per Expansion Card.) The 200-pin connector contacts are rated at 500 ma with a 30 degrees C rise. This number may have to be de-rated by some amount due to the environment of the card. The system supplying the power to the connector and cooling may also be a limiting factor. Voltage regulators limit some of the currents to below 500 ma.

Table 2.30 - 200-Pin Connector Power and Ground Pins

Voltage	No. of Pins	Max current
5	8	2 amps
3.3	20	3 amps
12	1	250 ma
AUX3.3	3	750 ma
GROUND	66	

At the I/O expansion card connector, Aux3.3v comes up first when the blade is plugged in. When the blade is powered on, 12v, 5v and 3.3v will begin to ramp up together. There is some delay between 12v, 5v and 3.3v, but it may not be fixed (i.e. the voltages are not sequenced). Once the voltages are at a good level, the Sys_Pwr_Gd signal is activated. Sys_Pwr_Gd activates about 200 ms after the voltages ramp up (200 ms is a minimum; there is no known maximum). The different power rails can come up in any sequence.

The tolerances on the 3.3V and 5V supplies are +/- 5%. The tolerance on the 12V supply is 12.2V +/- 3%. The new blade power designs are +/- 3% on 3.3V and 5V, but to work in all blades, the I/O Expansion Card must assume +/- 5%.

Over voltage (OV) protection is provided by the host system. Typical OV limits are as follows: +14.2V for 12V, +6.0V for 5V and +4.0V for 3.3V.

The above tolerances and over voltage protection values also apply to the High Speed I/O Expansion Cards described in Section 2.9.3.

2.9.2 I/O Expansion Card Power (CIOv)

The maximum power budget for the CIOv is 10 Watts/card (although the numbers in Table 2.25 add up to more than 10 W, the power usage is limited to 10W per Expansion Card.) The 160-pin connector contacts are rated at 1a with a 30 degrees C rise. This number may have to be de-rated by some amount due to the environment of the card. The system supplying the power to the connector and cooling may also be a limiting factor.

At the I/O expansion card connector, Aux3.3v comes up first when the blade is plugged in. When the blade is powered on, 5v and 3.3v will begin to ramp up together. There is some delay between 5v and 3.3v, but it may not be fixed (the voltages are not sequenced). Once the voltages are at a stable level, the POWERGOOD_CIOv signal is activated. POWERGOOD_CIOv activates about 200 ms after the voltages ramp up (200 ms is a minimum; there is no known maximum). The different power rails can come up in any sequence.

The tolerances are +/- 3% on 3.3V and 5V.

Over voltage (OV) protection is provided by the host system. Typical OV limits are +6.0V for 5V and +4.0V for 3.3V.

The maximum power budget for the CIOv I/O Expansion Cards is:

- CIOv: 10W

Although the numbers in Table 2.31 add up to more than 10W, the power usage is limited to the specified values per CIOv I/O Expansion Card.

Table 2.31 – CIOv I/O Expansion Card Power

Voltage	No. of Pins	Max current
3.3	4	4 amps
5	3	3 amps
AUX3.3	1	1 amp

The same tolerances apply to the CIOv I/O Expansion Cards as described in Section 2.9.1 for the I/O Expansion Cards.

2.9.3 High Speed I/O Expansion Card Power (HSEC, LFF HSEC, CFFh I/O Expansion Cards)

The maximum power budget for the High Speed I/O Expansion Cards is:

- HSEC: 15W
- LFF HSEC: 25W
- CFFh: 15W

Although the numbers in Table 2.32 add up to more than 25W, the power usage is limited to the specified values per High Speed I/O Expansion Card.

Table 2.32 - HSEC Power

Voltage	No. of Pins	Max current
3.3	8	3 amps
12	8	2.1 amps
AUX3.3	3	1 amp

The same tolerances apply to the High Speed I/O Expansion Cards as described in Section 2.9.1 for the I/O Expansion Cards.

2.10 Component Height Restrictions

The I/O expansion card design must not obstruct the airflow across the server blade. The component height restrictions will affect the use of heat sinks and should be a consideration in the overall design. The component height restrictions are shown in the chapter of Mechanical Drawings. For the CIOv Expansion Cards, the component height restrictions are included as part of the .emn mechanical kit file.

2.11 Thermal Design

Table 2.33 - Thermal Design of the I/O Expansion Card (EC)

	Enterprise	**Telco (NEBS)**
Airflow Velocity Bottom Side (closest to base planar)	50-150 LFM	50-150 LFM
Airflow Velocity Top Side	100-400 LFM	100-400 LFM
Maximum air temperature	52 ^{o}C	68 ^{o}C [2]
Minimum air temperature[1]	10 ^{o}C	-5 ^{o}C

[1] Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation will always be greater than these values.

[2] Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

Table 2.34 - Thermal Design of the CIOv I/O Expansion Card

	Enterprise	Telco (NEBS)
Airflow Velocity Bottom Side (closest to base planar)	TBD LFM	TBD LFM
Airflow Velocity Top Side	TBD LFM	TBD LFM
Maximum air temperature	TBD ^{o}C	TBD ^{o}C [2]
Minimum air temperature[1]	TBD ^{o}C	TBD ^{o}C

[1] Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation would always be greater than these values.

[2] Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

Table 2.35 - Thermal Design of the SFF I/O Expansion Card (SFF EC)

	Enterprise	Telco (NEBS)
Airflow Velocity Bottom Side (closest to base planar)	15-175 LFM	15-175 LFM
Airflow Velocity Top Side	15-400 LFM	15-400 LFM
Maximum air temperature	52 ^{o}C	68 ^{o}C [2]
Minimum air temperature[1]	10 ^{o}C	-5 ^{o}C

[1] Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation would always be greater than these values.

[2] Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

Table 2.36 - Thermal Design of the High Speed I/O Expansion Card (HSEC)

	Enterprise	Telco (NEBS)
Airflow Velocity Bottom Side (closest to base planar)[1]	150-400 LFM	175-450 LFM
Airflow Velocity Top Side [1]	250-800 LFM	285-910 LFM
Maximum air temperature	70 ^{o}C	60 ^{o}C (75 ^{o}C)[3]
Minimum air temperature[2]	10 ^{o}C	-5 ^{o}C

[1] Velocities are average local velocities, typically located at the inlet region to the card. Velocities inboard to the card will vary depending on component obstruction.

[2]Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation will always be greater than these values.

[3] Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

Table 2.37 - Thermal Design of the LFF High Speed I/O Expansion Card (LFF HSEC)

	Enterprise	Telco (NEBS)
Airflow Velocity Bottom Side (closest to base planar)[1,2]	250-600 LFM	285-685 LFM
Airflow Velocity Top Side [1,2]	450-700 LFM	510-800 LFM
Maximum air temperature	68 °C (68-85°C Max.)[4]	(63–80 Max.[4]) (78-95°C)[5]
Minimum air temperature[3]	10 °C	-5 °C

1 Velocities are average local velocities, typically located at the inlet region to the card. Velocities inboard to the card will vary depending on component obstruction.

2 Local velocity entering the center portion of the card can be as low as 50-80 LFM, from a near upstream heat sink obstruction. Careful attention should be given to placement of critical components.

3 Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation would always be greater than these values.

4 Maximum air inlet temperature will be concentrated at the center of the card. Attention to the placement of critical components should take this into account.

5 Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

CFFh I/O Expansion Card:
The Combo Form Factor H I/O Expansion Card (CFFh) follows same thermal requirements as defined by the High Speed I/O Expansion Card (HSEC).

Table 2.38 - Thermal Design of the CFFv I/O Expansion Card (CFFv)

	Enterprise	Telco (NEBS)
Airflow Velocity Bottom Side (closest to base planar)[1,2]	50-80 LFM	60-90 LFM
Airflow Velocity Top Side [1,2]	50-80 LFM	60-90 LFM
Maximum air temperature	(68-80 °C)[4] (85 °C Max.)[6]	(75-80 °C)[4] (85 °C)[5]
Minimum air temperature[3]	10 °C	-5 °C

1 Velocities are average local velocities, typically located at the inlet region to the card. Velocities inboard to the card will vary depending on component obstruction.

2 Local velocity entering the center portion of the card can be as low as 50-80 LFM, from a near upstream heat sink obstruction. Careful attention should be given to placement of critical components.

3 Minimum air temperature is per the enterprise and Telco operational specifications. Actual card temperature during operation would always be greater than these values.

4 Maximum air inlet temperature will be concentrated at the center of the card. Attention to the placement of critical components should take this into account.

5 Maximum air temperature for short term temperature excursion of 96 hours or less, per the NEBS compliancy specification.

6 Maximum air temperature for cooling redundancy mode. Recommended not to exceed 24 hours.

2.12 I^2C (VPD) Interface

The I/O Expansion Card supports an I^2C interface on the 200-pin or 450-pin connector. The I/O Expansion Card must provide a 24C64 64Kbit (8Kx8) Serial EEPROM for system Vital Product Data (VPD), or equivalent data structure up to 128Kbit. This interface supports the Atmel AT24C64N-10SIC-1.8 and STMicro M24C64 WMN6 or equivalent. It is only accessible by the BMC via an I^2C bus. This part is located at system address hex "**0xA2**" for HSDC expansion cards, and **"0xA0"** for the CIOv, EC, SFF EC, and CFFv xpansion cards. The 24C64 obtains its power from AUX3.3V.

For HSEC designs that utilize chipsets on both the "B" bus and the "A" bus, a separate VPD device must be attached to each applicable VPD segment on the HSEC connector.

2.13 VPD

Each I/O Expansion Card subsystem must include Vital Product Data (VPD) information that is accessed by the chassis management module via the Blade Service Processor. For details, see the Base Specification for VPD.

2.14 Optional Temperature Reporting

The I/O Expansion Card may optionally contain temperature sensors. For guidelines on sensor placement and data reporting, see the BladeServer Base Specification For Processor Blade Subsystems.

2.15 I/O Expansion Card Detection of BladeCenter Chassis and Slot

The I/O Expansion Card can implement an optional I2C Port Expander to be informed by the Blade Service Processor exactly which chassis type and BladeServer slot the expansion card installs into within the chassis.

Hardware requirements

- I/O Expansion card must add an 8-bit I2C port expander for the BladeServer to access in order for the Blade Service Processor to access on auxiliary power.
- Fixed I2C address of D0h for powered by 3.3v AUX (suggested part is MAX7321).
- VPD must reflect I2C port expander is present. Refer to VPD Base Specification in the Capabilities Field for specific details.

Software requirements

- I/O Expansion card must access the 8-bit output of the I2C port expander directly. The I/O Expansion card must not access the I2C port expander over the I2C bus.

The 8-bits provide both the chassis type and the slot information. There are 4 bits for the chassis encode, and 4 bits for the slot encode.

Table 2.39 - Chassis type and slot information

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slot ID Bit 3	Slot ID Bit 2	Slot ID Bit 1	Slot ID Bit 0	Chassis ID Bit 3	Chassis ID Bit 2	Chassis ID Bit 1	Chassis ID Bit 0
Slot ID				Chassis ID			

Table 2.40 - Chassis and Slot Encoding

Chassis Type (bits 3-0)	Slot Position (bits 7-4)
0000b = Reserved	0000b = Reserved
0001b = Reserved	0001b = Slot 1
0010b = Reserved	0010b = Slot 2
0011b = Reserved	0011b = Slot 3
0100b = BCE	0100b = Slot 4
0101b = Reserved	0101b = Slot 5
0110b = BCH	0110b = Slot 6
0111b = BCS	0111b = Slot 7
1000b = BCT	1000b = Slot 8
1001b = Reserved	1001b = Slot 9
1010b = BCHT	1010b = Slot 10
1011b = Reserved	1011b = Slot 11
1100b = Reserved	1100b = Slot 12
1101b = Reserved	1101b = Slot 13
1110b = Reserved	1110b = Slot 14
1111b = Unknown	1111b = Reserved

3 Mechanical Design

This section will provide mechanical card and connector information for the seven I/O Expansion Card types.

3.1 I/O Expansion Card Mechanical Design Kits

I/O Expansion Card Mechanical Design Kits are available at the following URL:

http://www-03.ibm.com/systems/bladecenter/open_specs.html.

Mechanical Design Kits provide data necessary to design the printed circuit card for the I/O Expansion Cards. They also provide definition of mechanical hardware needed on the I/O Expansion Cards. The mechanical design kit consists of a "Readme" file, a set of 3D CAD models, and PDF files which provide a base for designing an I/O Expansion Card. The 3D CAD models are in Pro/ENGINEER Wildfire 2.0® design software, IGES, STEP, and an EMN file format. The EMN file of the printed circuit card will define the card outline, connector location, component keep-out areas and component height restrictions. The 2D drawings are provided in Adobe® PDF file format. A bill of material is included in the design kit "Readme" file. The mechanical design information in the design kits shall take precedence over the following information. Information describing 240 VA keep-out areas is stated exclusively in this document, not in the Mechanical Design Kits.

3.2 Mechanical Design Notes

The following notes pertain to all card types. The cards must meet National and International applicable safety and marketing requirements such as, but not limited to, 240VA limiting and EMC and ESD Standards.

Notes:

1) All non-plated holes to have a tolerance of +/- 0.076mm (0.003") unless otherwise stated. Linear tolerance of +/- 0.076mm (0.003") for routed and hole location dimensions. All others to be +/- 0.25mm (0.010")

2) No components shall protrude past the edge of the card unless noted on the drawing.

3) If a cable is required to interface with this card it must exit within the indicated area. The cable connector must not protrude past the edge of the card.

4) No components, connectors or cables may violate the component height restrictions.

5) The installation label is required on cards as noted on the drawings

6) After soldering all connectors must be flush to 0.127mm (0.005") to the card surface.

7) Maximum weight of the I/O expansion cards are not to exceed as follows:

I/O Expansion Card (EC) Assembly	55 grams (0.12 lbs.)
SFF I/O Expansion Card (SFF EC) Assembly	55 grams (0.12 lbs.)
High Speed I/O Expansion Card (HSEC) Assembly	TBD grams (TBD lbs.)
LFF High Speed I/O Expansion Card (LFF HSEC) Assembly	TBD grams (TBD lbs.)

CFFv I/O Expansion Card (CFFv) Assembly	55 grams (0.12 lbs.)
CFFh I/O Expansion Card (CFFh) Assembly	114 grams (0.25 lbs.)
CIOv I/O Expansion Card (CIOv) Assembly	TBD grams (TBD lbs.)

The following drawings apply to an I/O expansion card designed specifically to attach to a BladeServer standard Blade. The mechanical design may be used "as is" on other Blades but the designer must ensure that the location of the card does not compromise the thermal performance of the Blade and that any mechanical means of retaining the card contact the indicated component free areas only.

Figures 3.1 through 3.6 are the mechanical drawings for the I/O Expansion Card (EC).
Figures 3.7 through 3.12 are the mechanical drawings for the Small Form Factor I/O Expansion Card (SFF EC).
Figures 3.13 through 3.18 are the mechanical drawings for the Large Form Factor High Speed I/O Expansion Card (LFF HSEC).
Figures 3.19 through 3.24 are the mechanical drawings for the High Speed I/O Expansion Card (HSEC)
Figures 3.25 through 3.30 are the mechanical drawings for the CFFh I/O Expansion Card (CFFh)
Figures 3.31 through 3.36 are the mechanical drawings for the CFFv I/O Expansion Card (CFFv)
Figures 3.37 through 3.40 are the preliminary mechanical drawings for the CIOv I/O Expansion Card (CIOv)

The label shown in Figure 3.1 is used to indicate where to push on the card during installation and shall say "PRESS TO INSTALL".

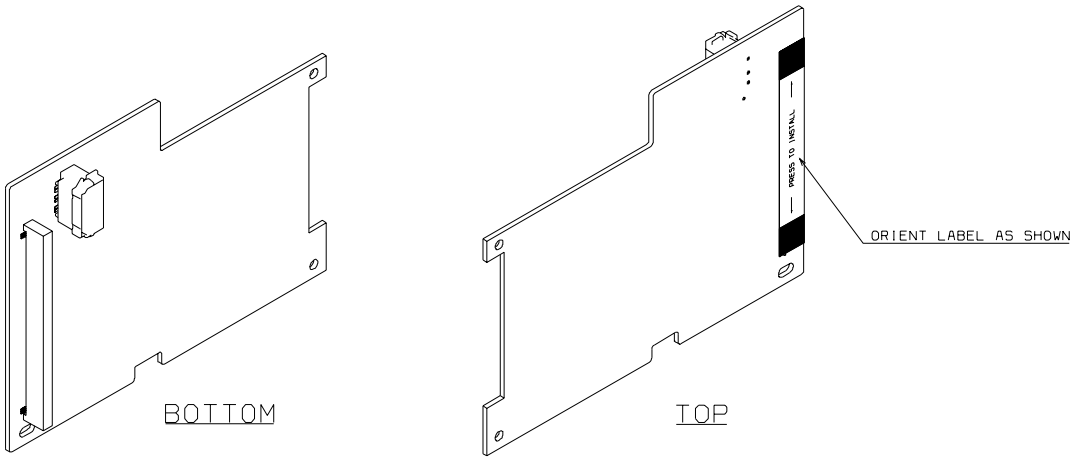


Figure 3.1. I/O Expansion Card (EC) - isometric views

The card thickness defined in Figure 3.2 is for reference only and may vary depending on the application.

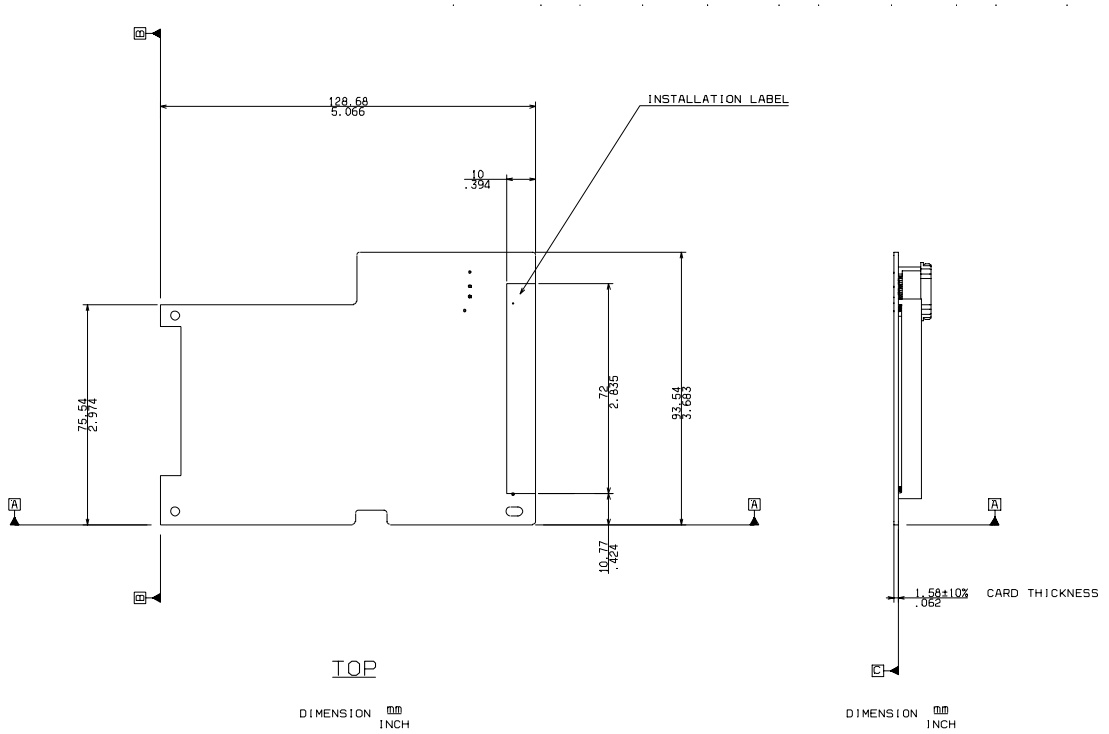
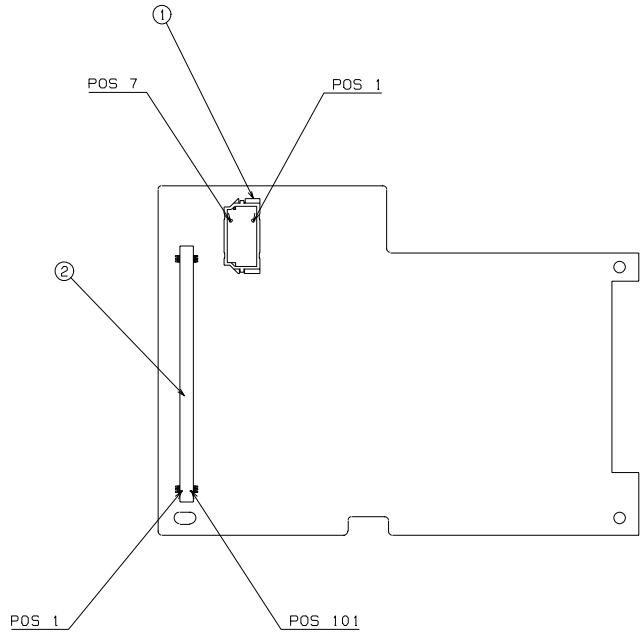


Figure 3.2. I/O Expansion Card (EC) - top and side views



Item	Description	Reference
Item 1	High Speed Connector	Refer to Table 2.4
Item 2	PCI Interface Connector (2 X 100)	Refer to Table 2.1

Figure 3.3. I/O Expansion Card (EC) - bottom view – connector and pin definition

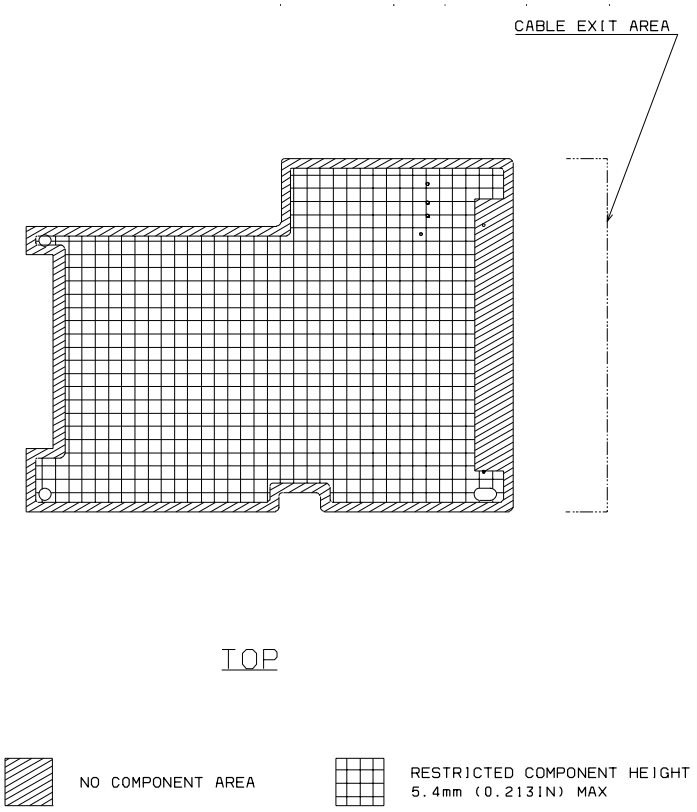


Figure 3.4. I/O Expansion Card (EC) – top view – component height restrictions

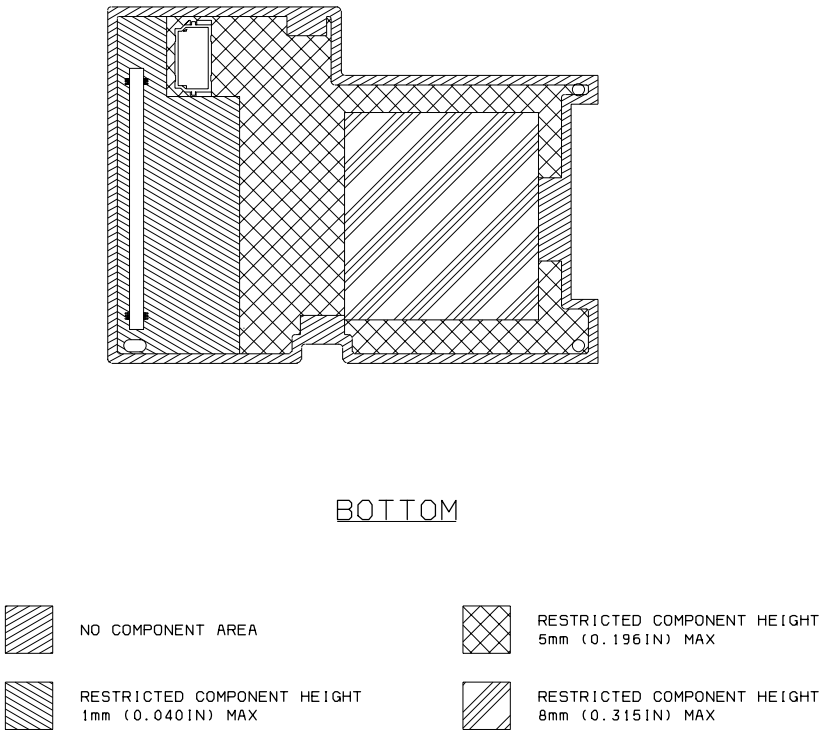


Figure 3.5. I/O Expansion Card (EC) – bottom view – component height restrictions

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may, in some cases, short.

The area defined in Figure 3.6 must be free of exposed 240 VA circuits.

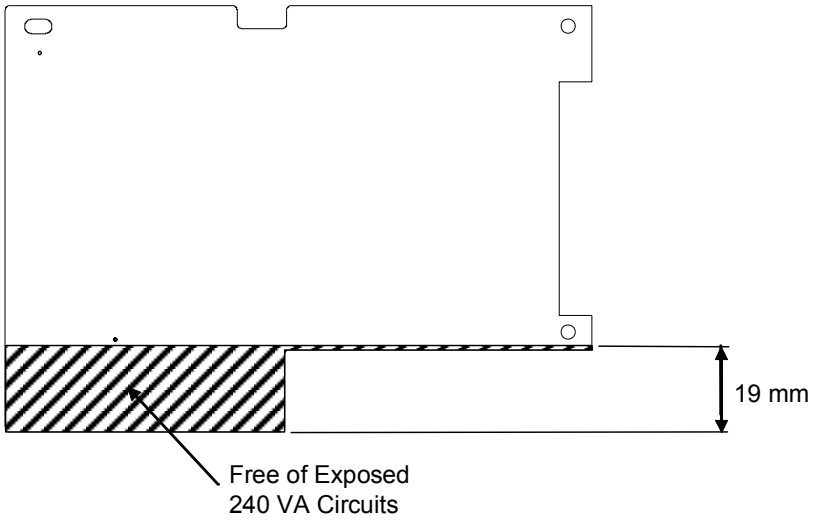


Figure 3.6. I/O Expansion Card (EC) – top view – 240 VA circuit keep-out area

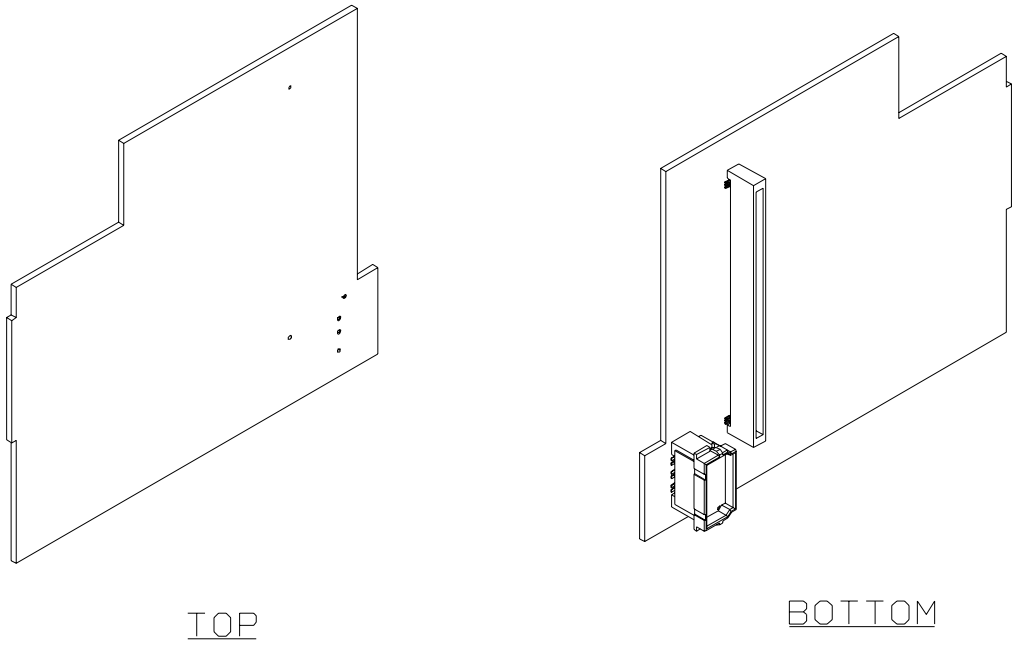


Figure 3.7. Small Form Factor I/O Expansion Card (SFF EC) – isometric views

The label shown in Figure 3.8 is used to indicate where to push on the card during installation and shall say "PRESS TO INSTALL".

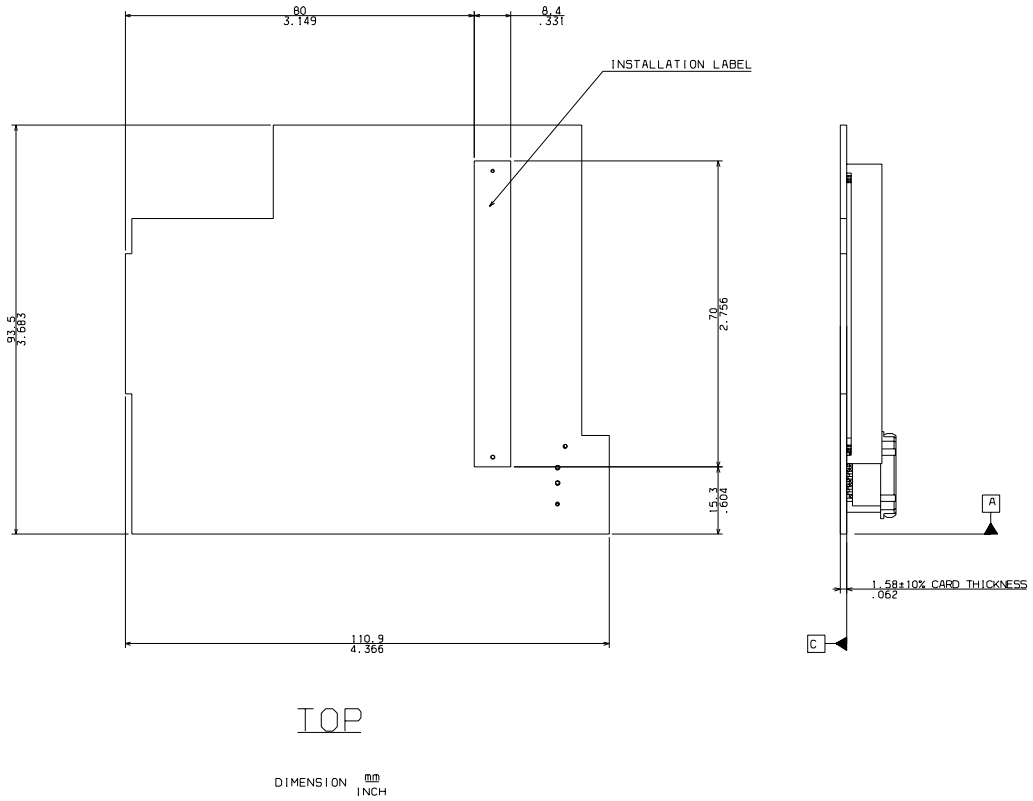
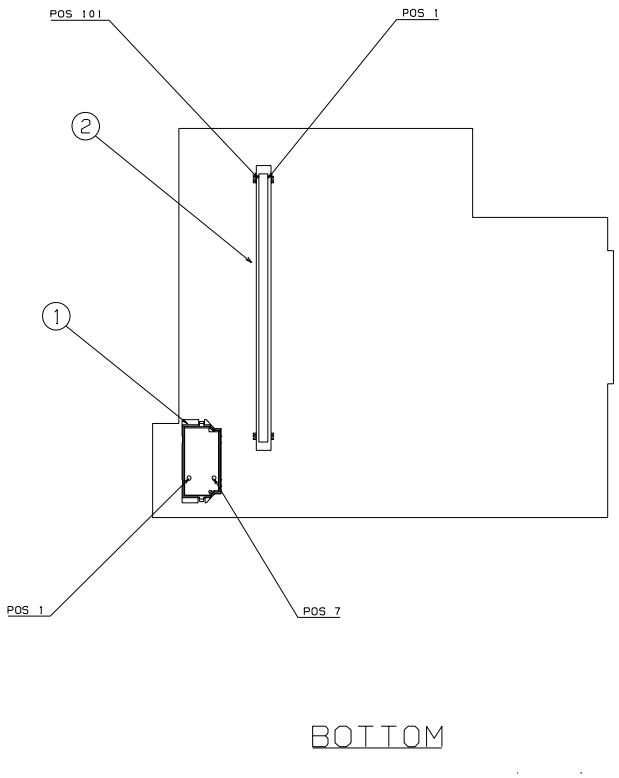


Figure 3.8. Small Form Factor I/O Expansion Card (SFF EC) – top view – card size, installation label



Item	Description	Reference
Item 1	High Speed Connector	Refer to Table 2.4
Item 2	PCI Interface Connector (2 X 100)	Refer to Table 2.1

Figure 3.9. Small Form Factor I/O Expansion Card (SFF EC) – bottom view – connectors and pin definition

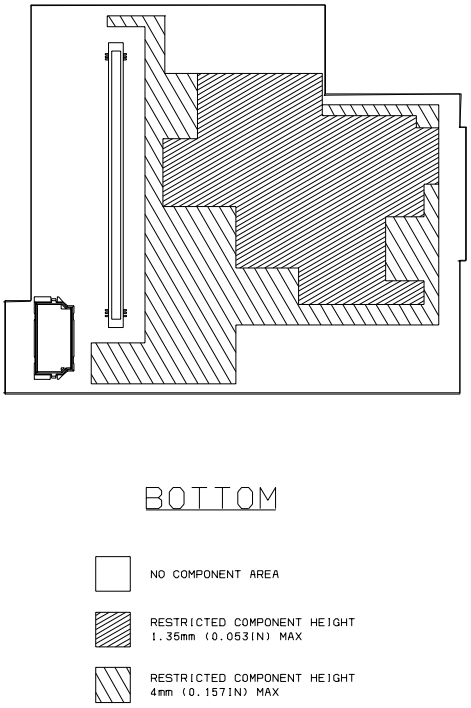


Figure 3.10. Small Form Factor I/O Expansion Card (SFF EC) – bottom view – component height restrictions

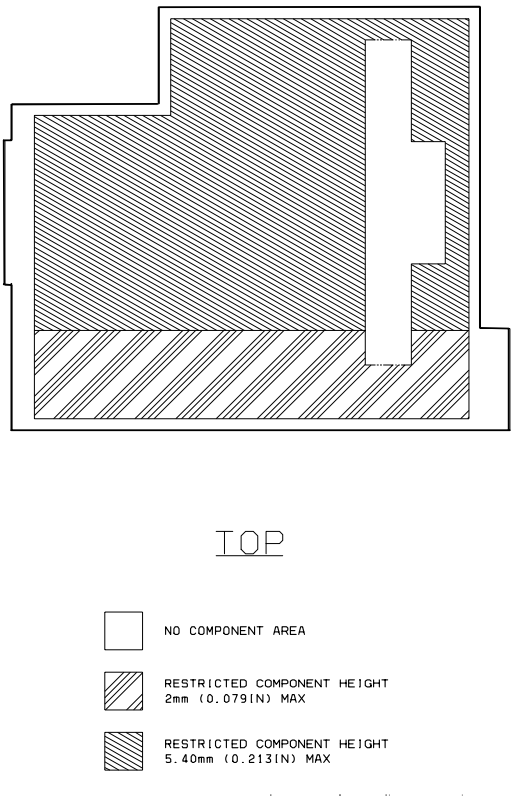


Figure 3.11. Small Form Factor I/O Expansion Card (SFF EC) - top view - component height restrictions

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may, in some cases, short.

The area defined in Figure 3.12 must be free of exposed 240 VA circuits.

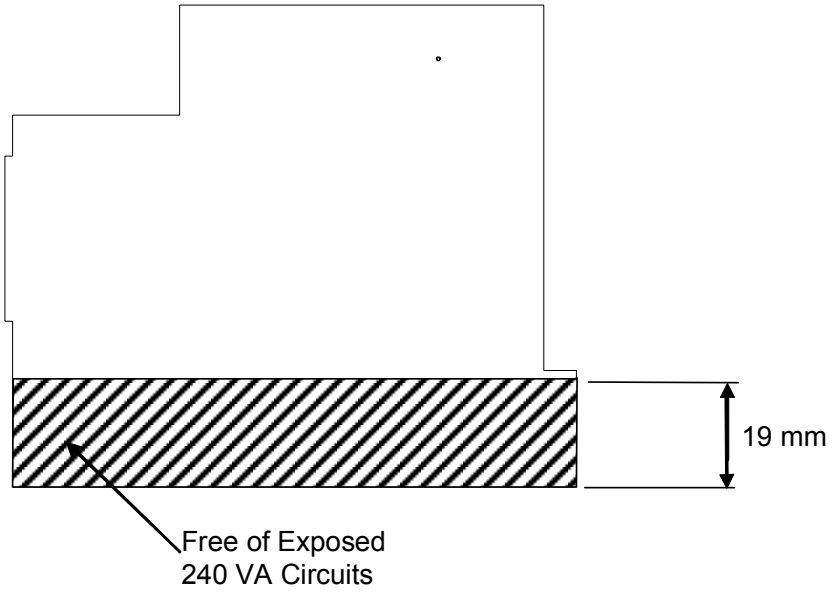


Figure 3.12. Small Form Factor I/O Expansion Card (SFF EC) – top view – 240 VA circuit keep-out area

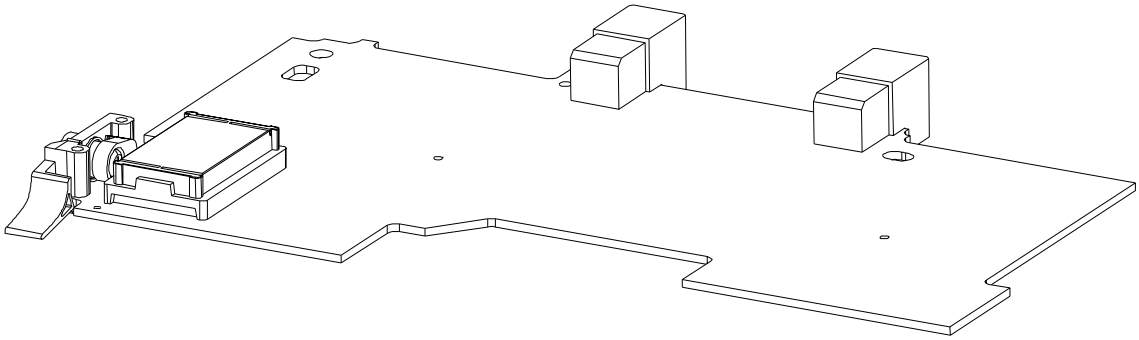
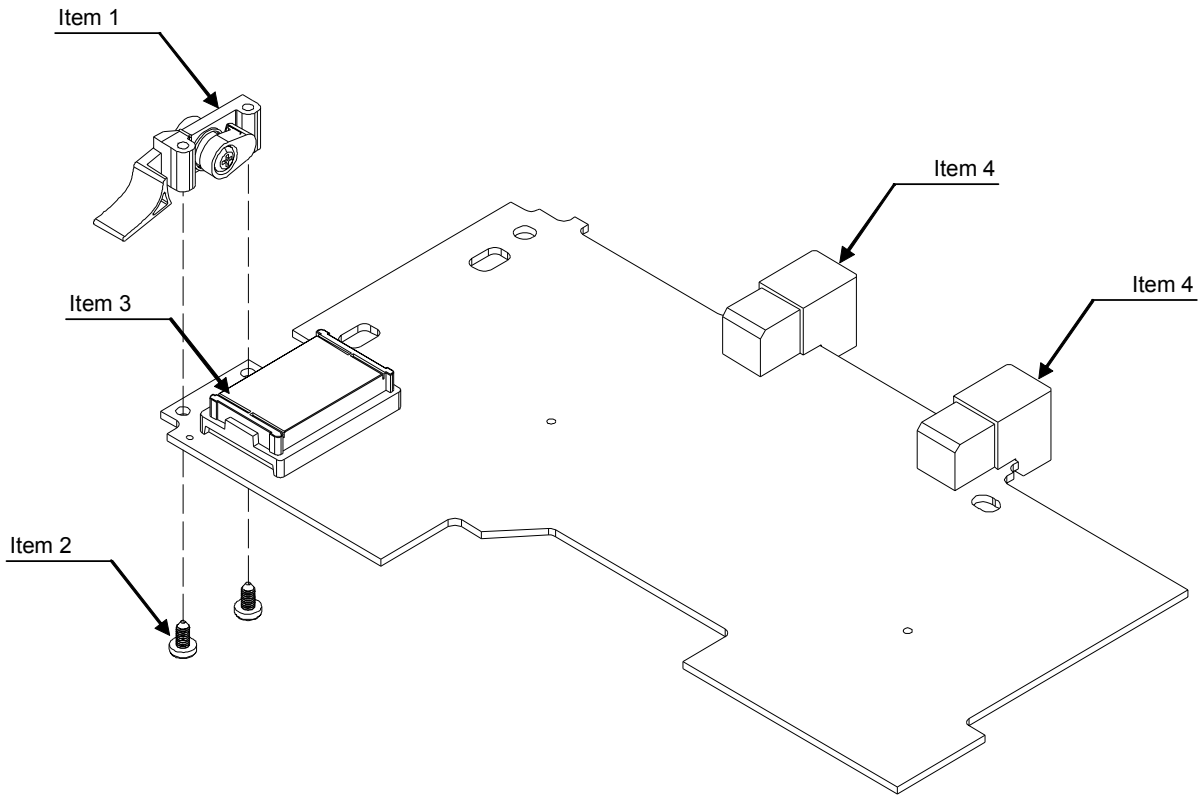
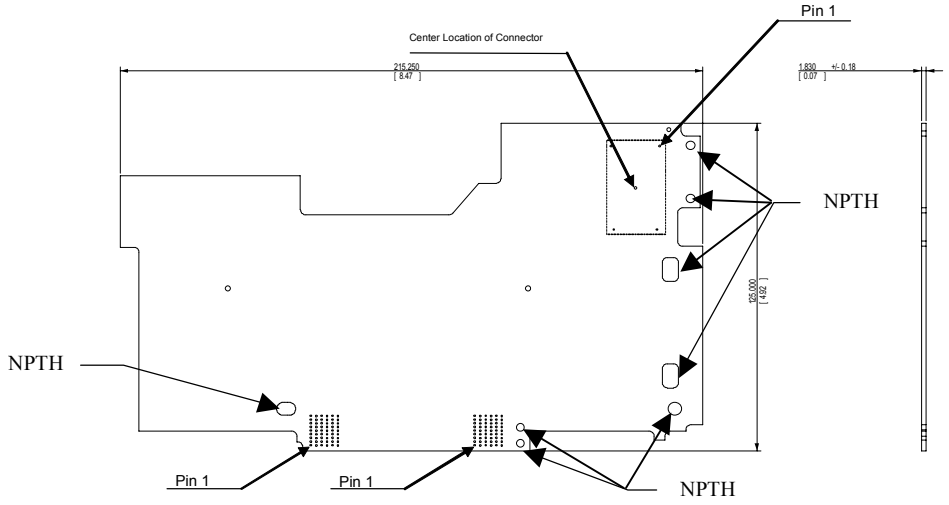


Figure 3.13. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – bottom isometric view



Item	Description	Reference
Item 1	Lever	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 2	Screw	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 3	PCI-Express Interface Connector	Refer to Table 2.6
Item 4	Midplane Connector	Refer to Table 2.18

Figure 3.14. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – bottom isometric view – exploded



Note: Holes/Slots marked with NPTH are not required to be plated holes because they interface with non-conductive plastic hardware.

Figure 3.15. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – bottom view – card size, connector / module locations

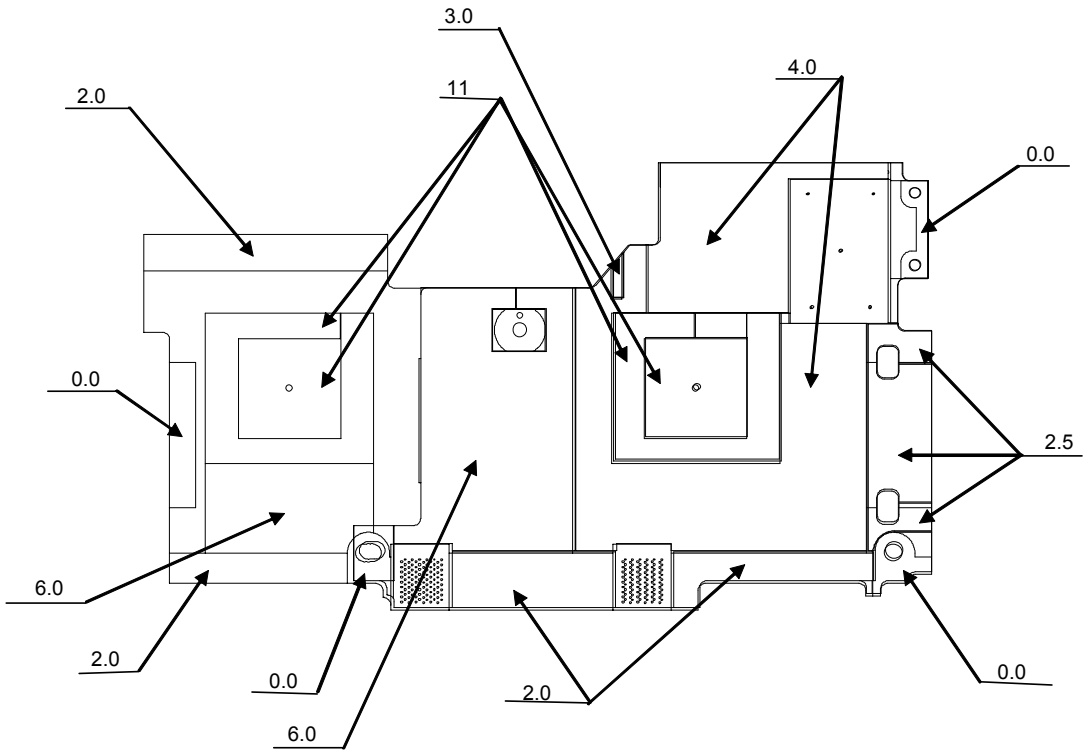


Figure 3.16. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – bottom view – component height restrictions (heights in mm)

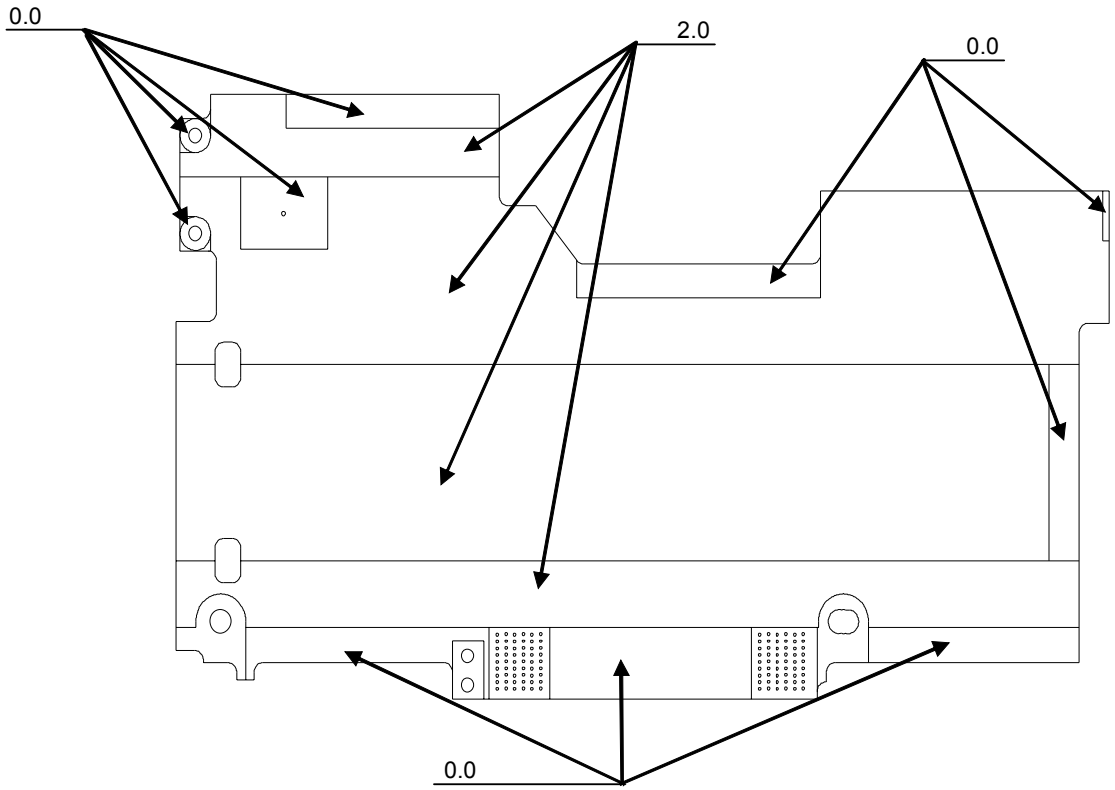


Figure 3.17. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – top view – component height restrictions (heights in mm)

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may in some cases short.

The area defined in Figure 3.18 must be free of exposed 240 VA circuits.

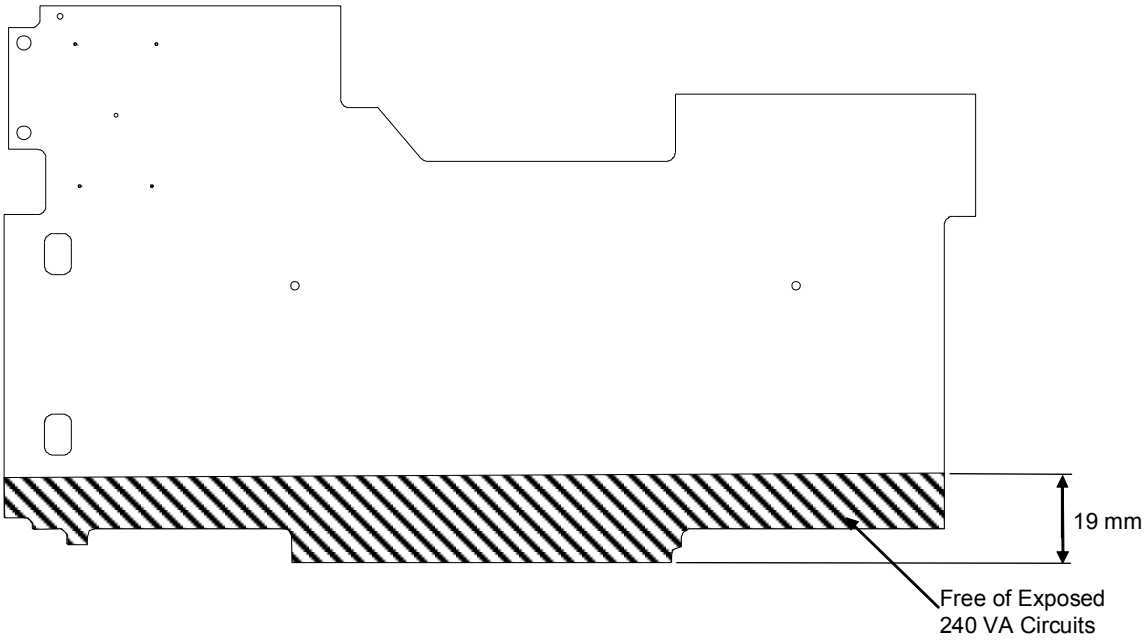


Figure 3.18. Large Form Factor High Speed I/O Expansion Card (LFF HSEC) – top view – 240 VA circuit keep-out area

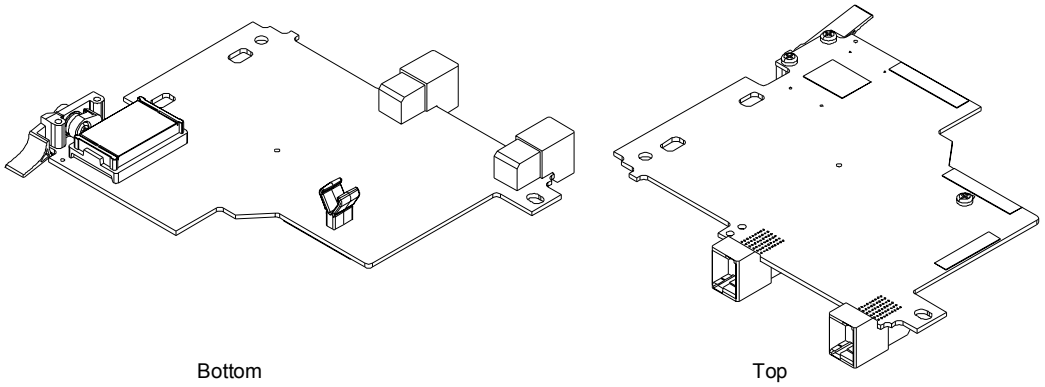
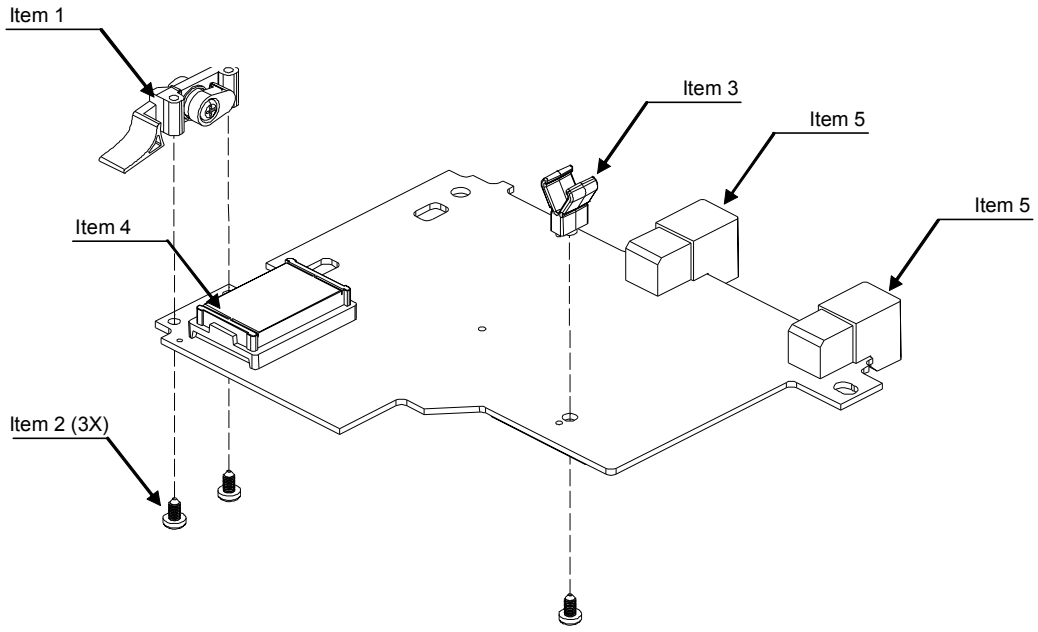
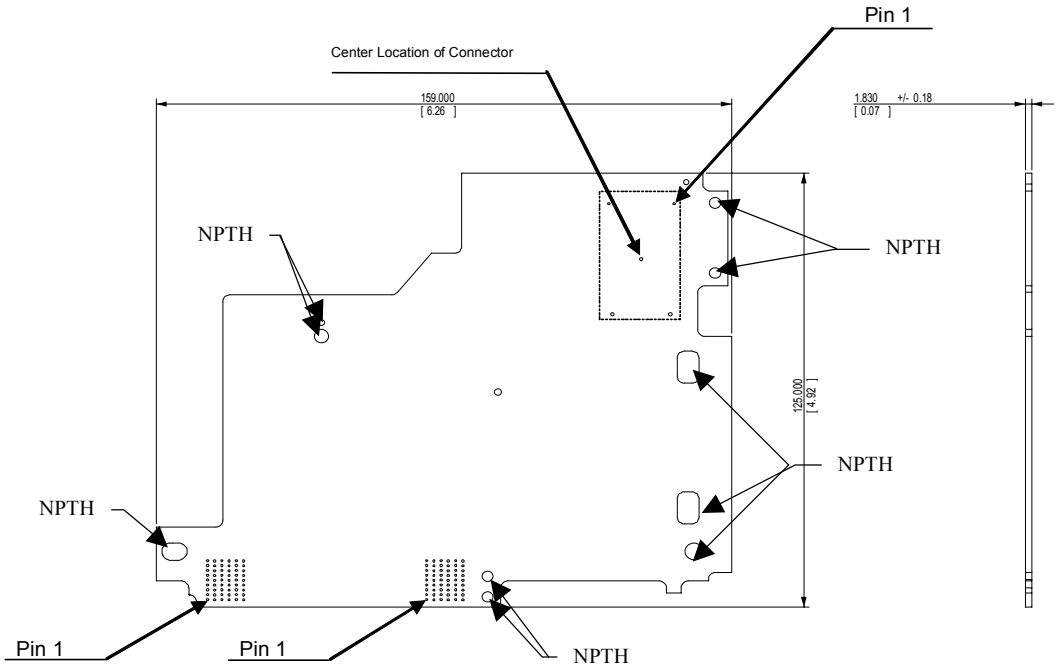


Figure 3.19. High Speed I/O Expansion Card (HSEC) –isometric views



Item	Description	Reference
Item 1	Lever	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 2	Screw	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 3	Snap	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 4	PCI-Express Interface Connector	Refer to Table 2.6
Item 5	Midplane Connector	Refer to Table 2.20

Figure 3.20. High Speed I/O Expansion Card (HSEC) – bottom isometric view – exploded



Note: Holes/Slots marked with NPTH are not required to be plated holes because they interface with non-conductive plastic hardware.

Figure 3.21. High Speed I/O Expansion Card (HSEC) – bottom view – card size, connector / module locations

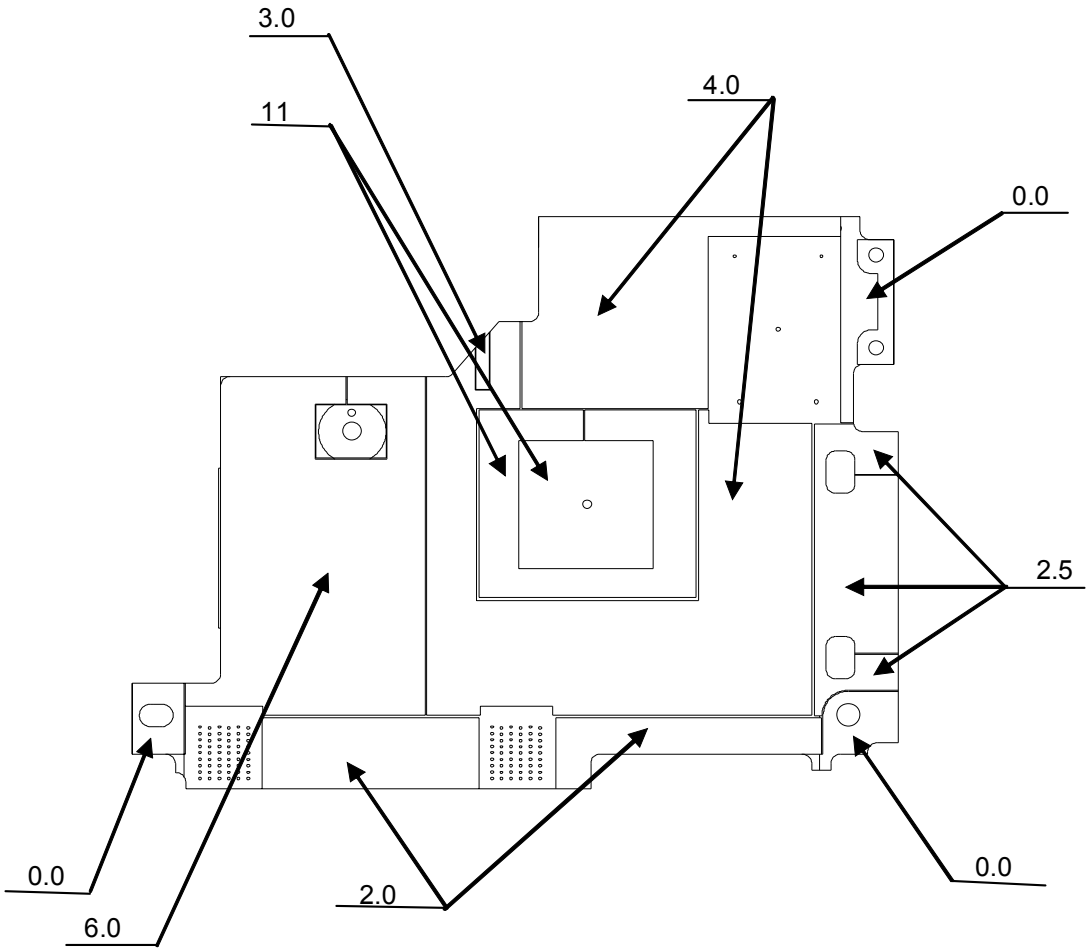


Figure 3.22. High Speed I/O Expansion Card (HSEC) – Bottom View – component height restrictions (heights in mm)

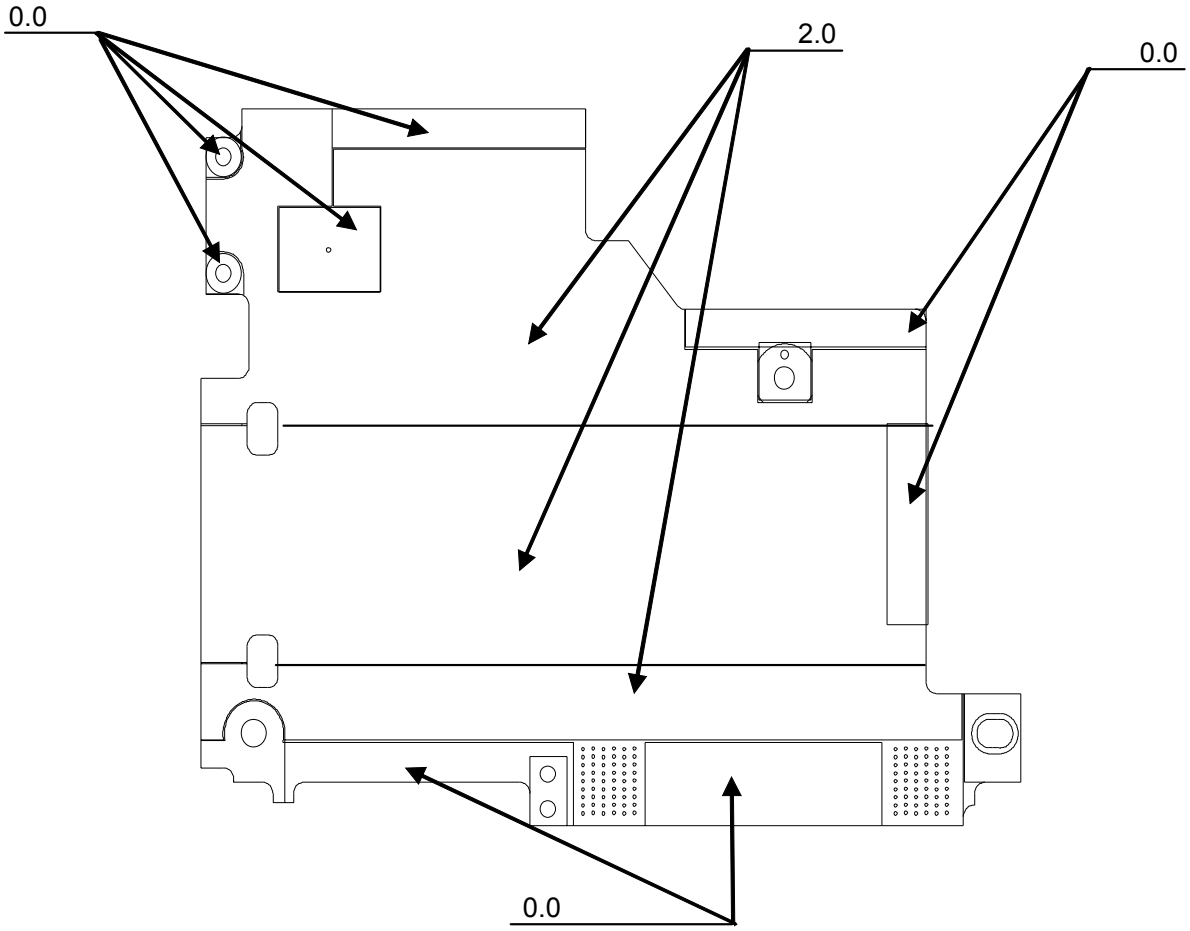


Figure 3.23. High Speed I/O Expansion Card (HSEC) – top view – component height restrictions (heights in mm)

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may in some cases short.

The area defined in Figure 3.24 must be free of exposed 240 VA circuits.

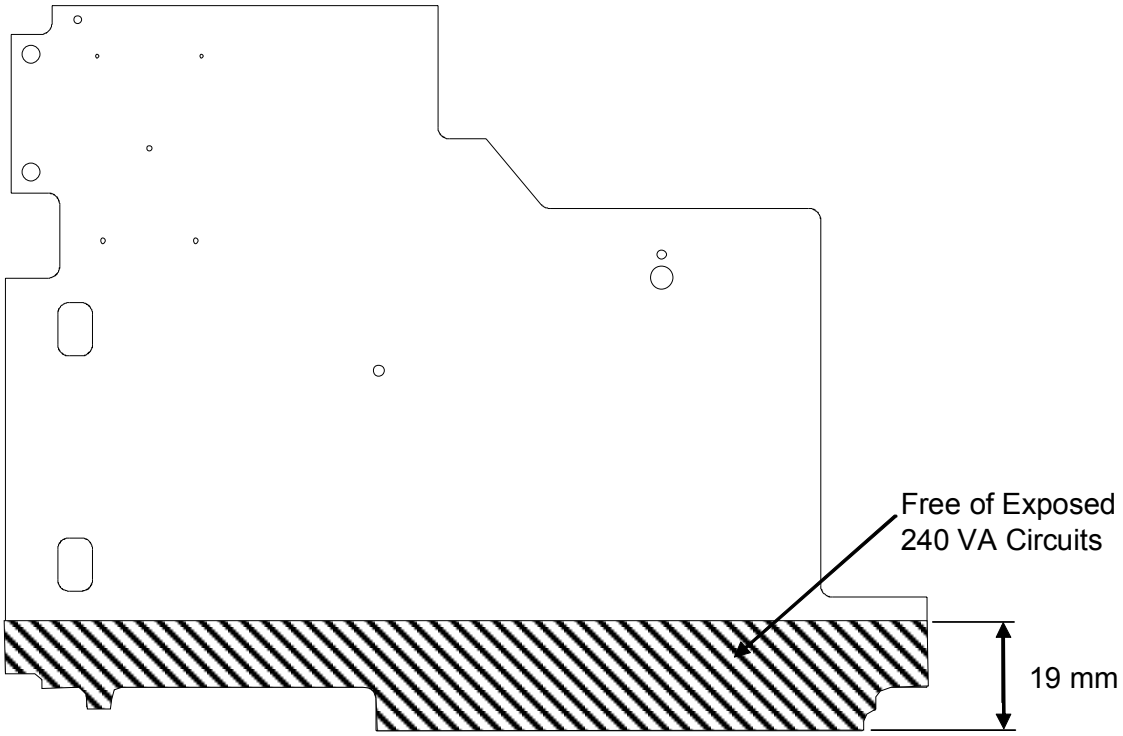


Figure 3.24. High Speed I/O Expansion Card (HSEC) – top View – 240 VA circuit keep-out area

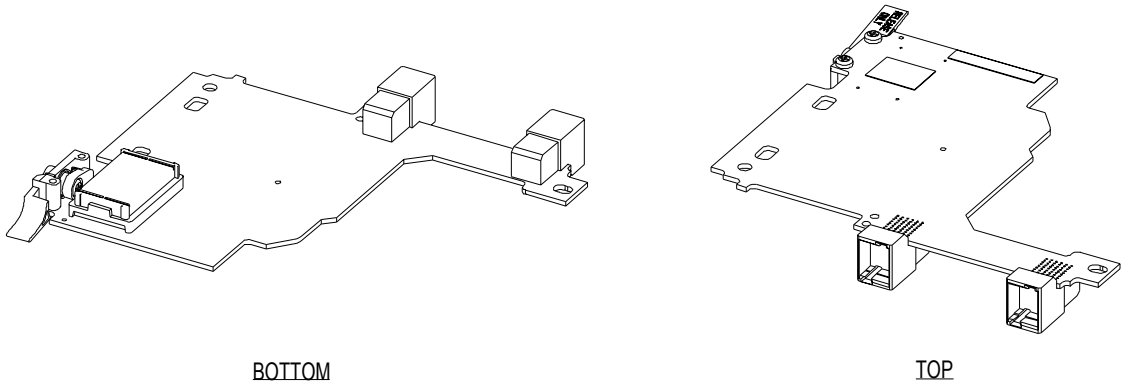
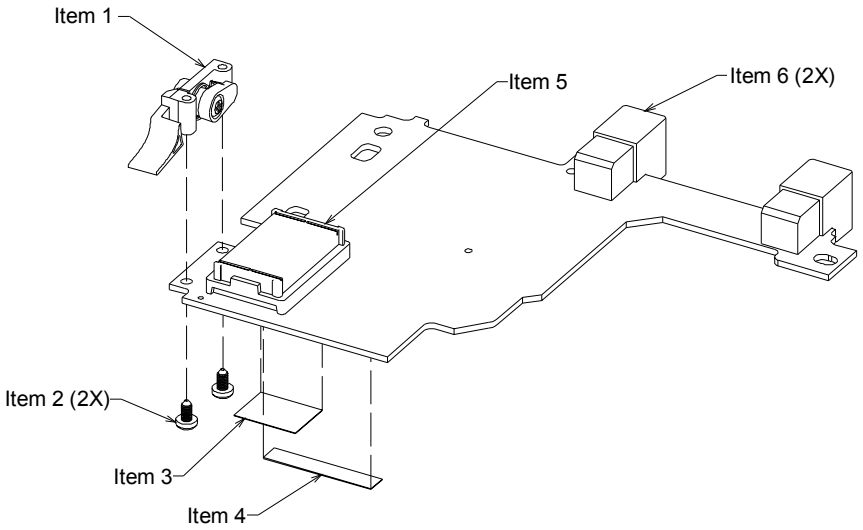
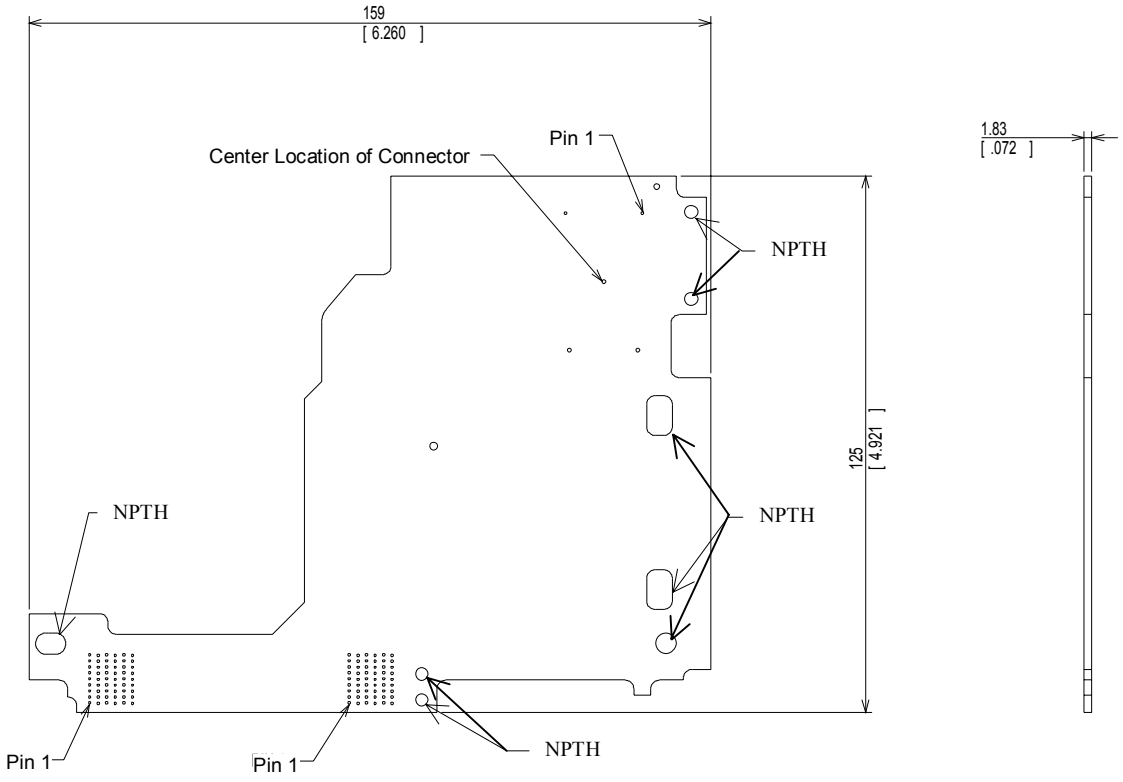


Figure 3.25. CFFh I/O Expansion Card (CFFh) – isometric views



Item	Description	Reference
Item 1	Lever	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 2	Screw	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 3	Label, “Press to Install”	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 4	Serialized Barcode Label	
Item 5	PCI-Express Interface Connector	Refer to Table 2.6
Item 6	Midplane Connector	Refer to Table 2.20

Figure 3.26. CFFh I/O Expansion Card (CFFh) – isometric views



Note: Holes/Slots marked with NPTH are not required to be plated holes because they interface with non-conductive plastic hardware.

Figure 3.27. CFFh I/O Expansion Card (CFFh) – bottom view – card size, connector / module locations

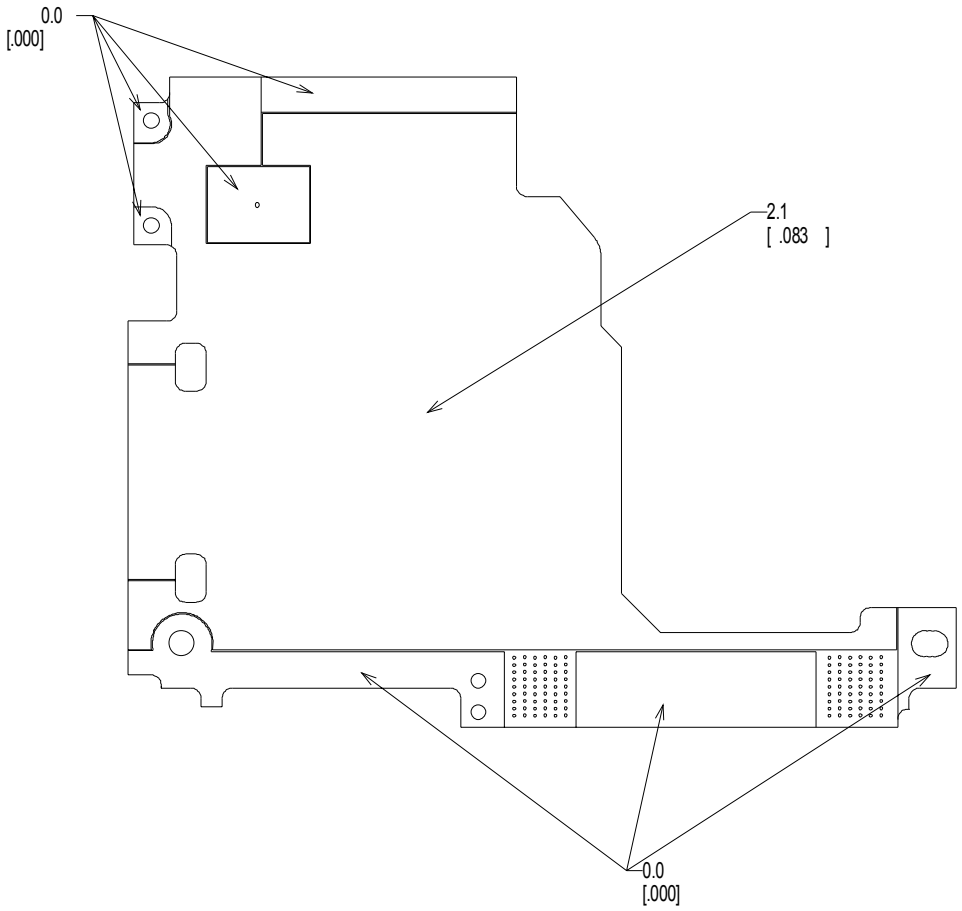


Figure 3.28. CFFh I/O Expansion Card (CFFh) – top view – component height restrictions (heights in mm [in.])

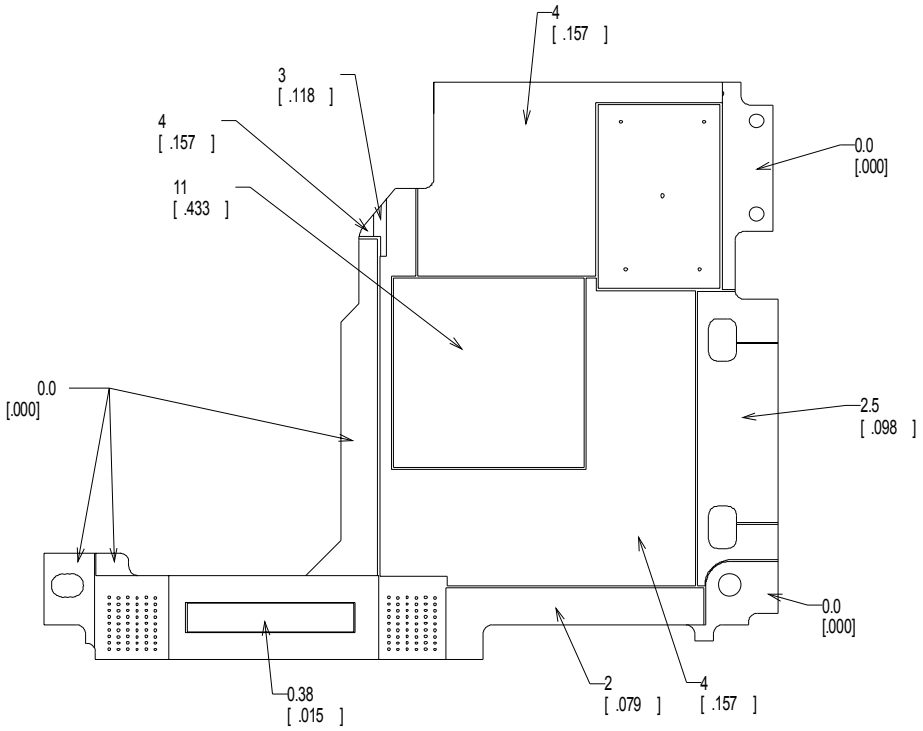


Figure 3.29. CFFh I/O Expansion Card (CFFh) – bottom view – component height restrictions (heights in mm [in.])

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may in some cases short.

The area defined in Figure 3.30 must be free of exposed 240 VA circuits.

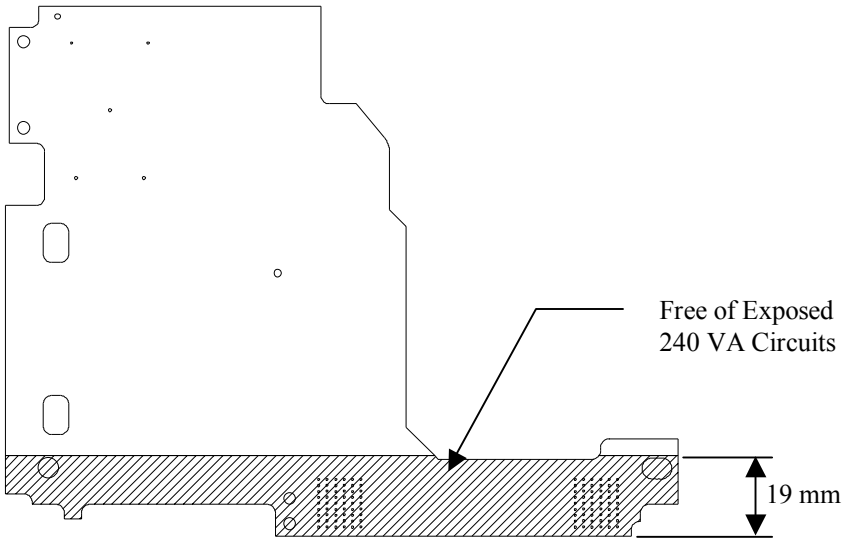


Figure 3.30. CFFh I/O Expansion Card (CFFh) – top view – 240 VA circuit keep-out area

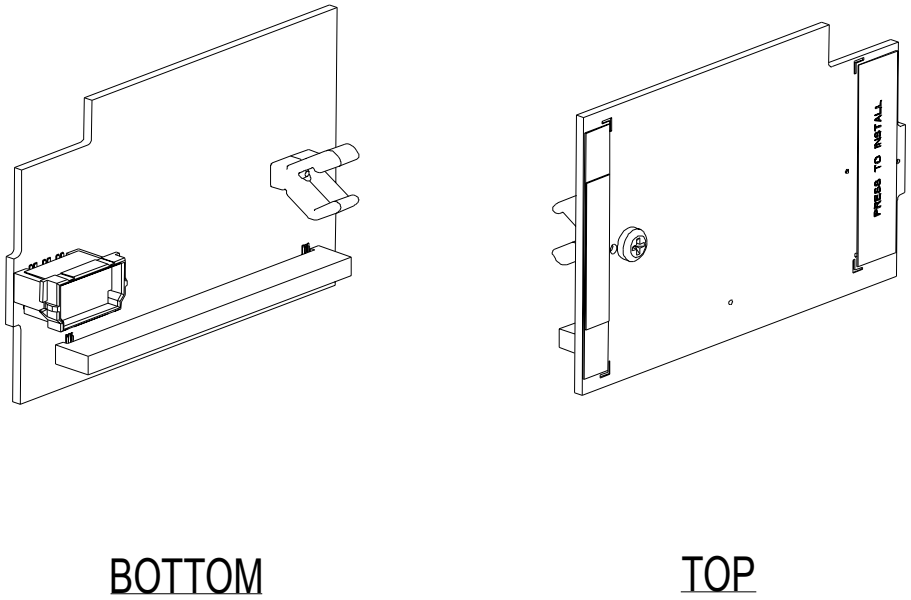
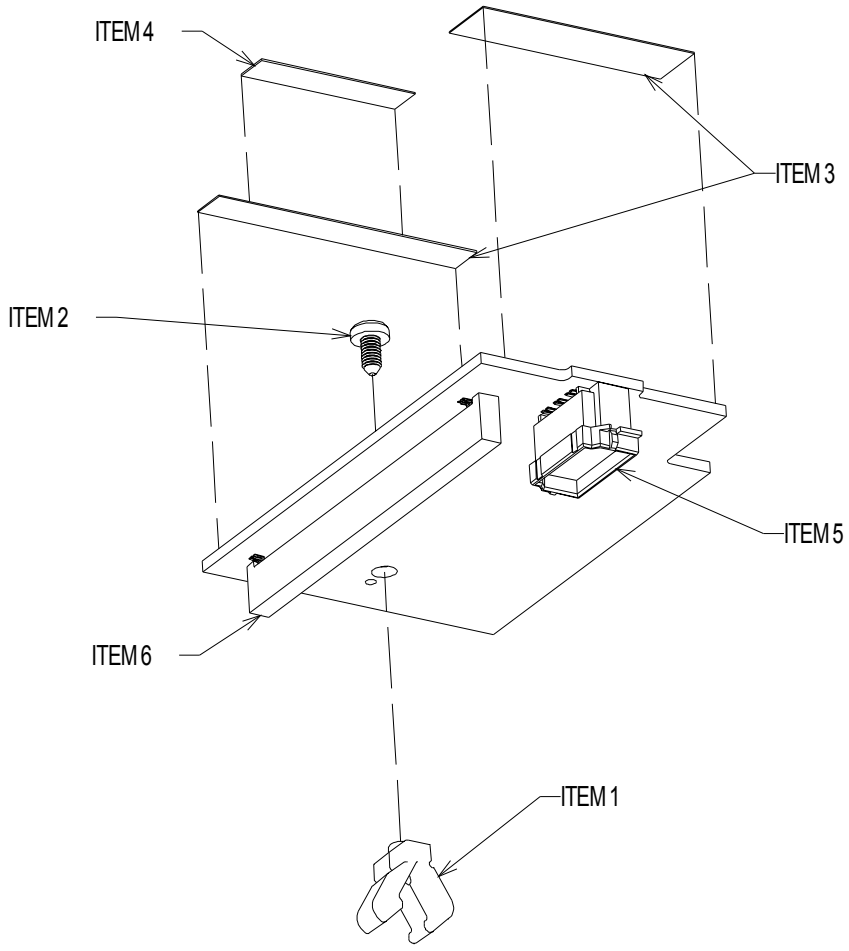
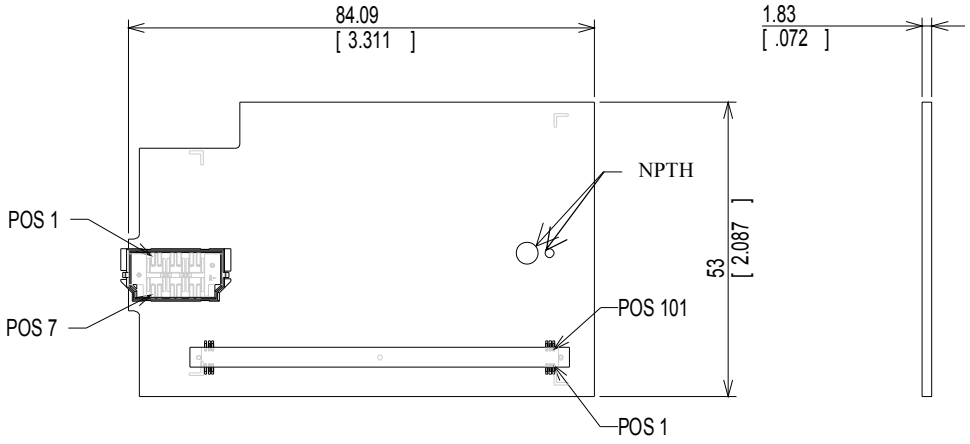


Figure 3.31. CFFv I/O Expansion Card (CFFv) – isometric views



Item	Description	Reference
Item 1	Snap	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 2	Screw	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 3	Label, “Press to Install”	Refer to associated I/O Expansion Card Mechanical Design Kit
Item 4	Serialized Barcode Label	
Item 5	High Speed Connector	Refer to Table 2.4
Item 6	PCI Interface Connector (2x100)	Refer to Table 2.1

Figure 3.32. CFFv I/O Expansion Card (CFFv) – angled view - exploded



Note: Holes/Slots marked with NPTH are not required to be plated holes because they interface with non-conductive plastic hardware

Figure 3.33. CFFv I/O Expansion Card (CFFv) – bottom view – card size, connector / module locations

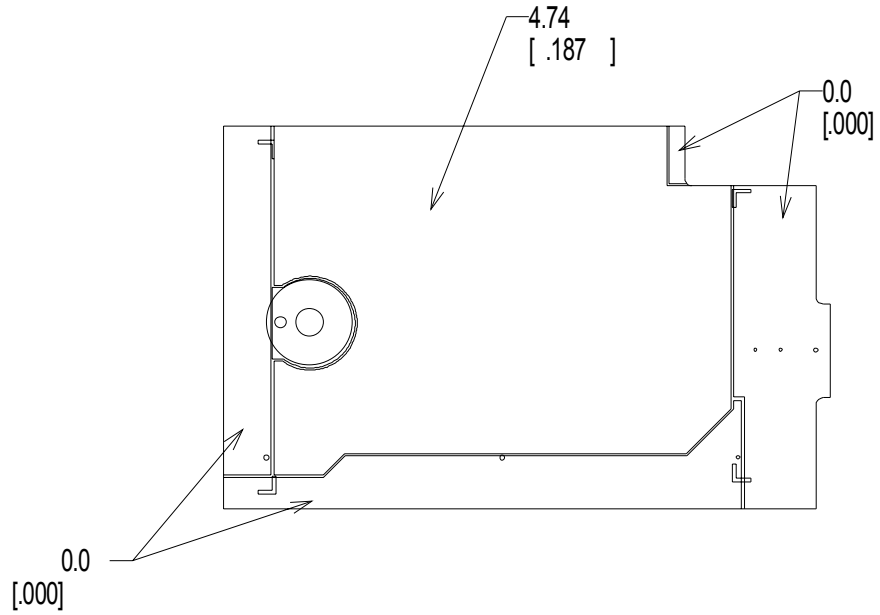


Figure 3.34. CFFv I/O Expansion Card (CFFv) – top view – component height restrictions (heights in mm [in.])

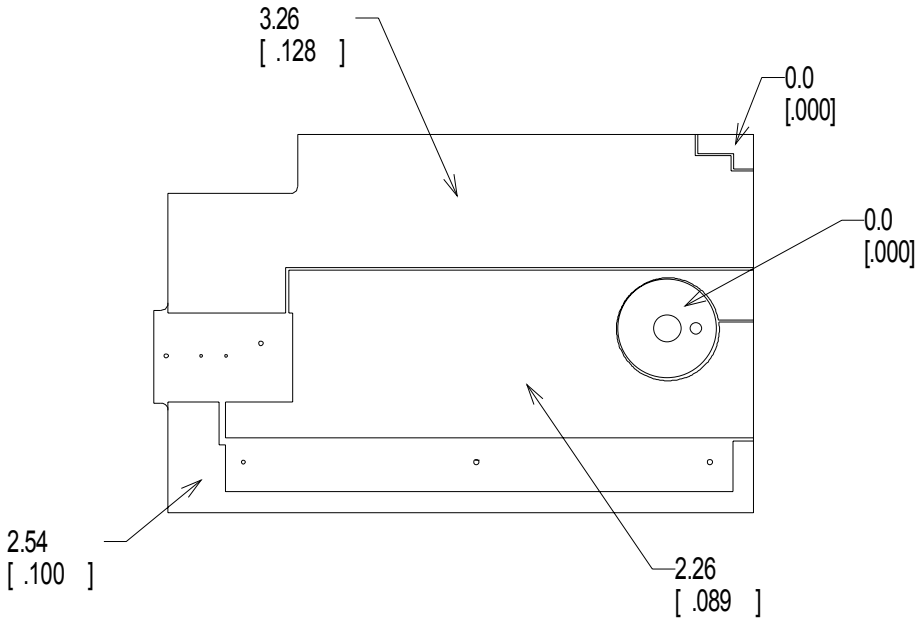


Figure 3.35. CFFv I/O Expansion Card (CFFv) – top view – component height restrictions (heights in mm [in.])

There may be conductive surfaces adjacent to the maximum heights of the keep-out areas. Proper insulation must be provided on those components that may be at a potential different than ground and therefore may in some cases short.

The area defined in Figure 3.36 must be free of exposed 240 VA circuits.

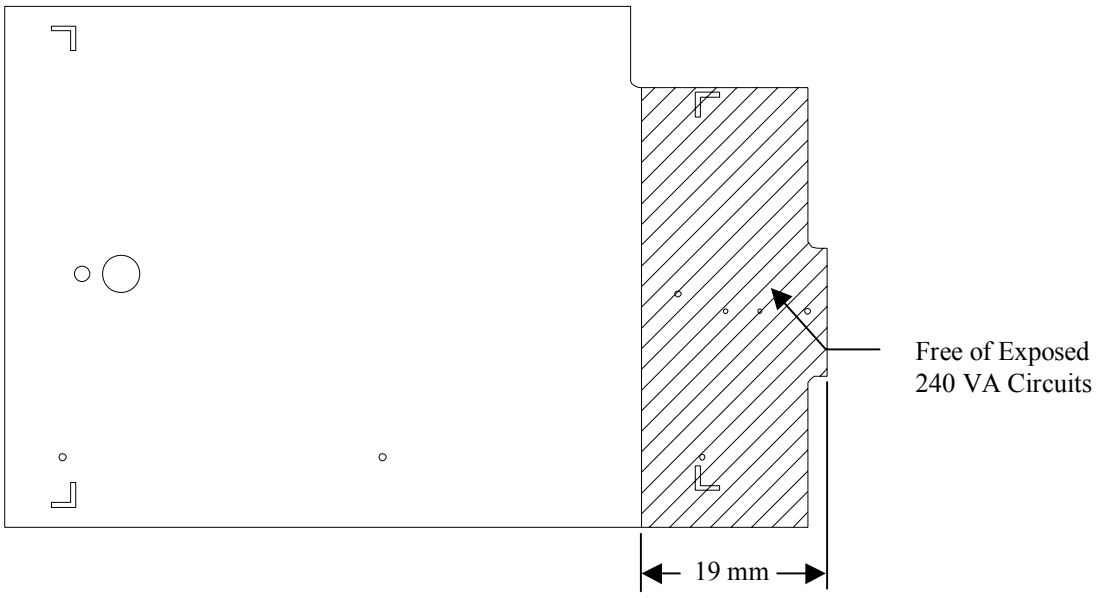


Figure 3.36. CFFv I/O Expansion Card (CFFv) – top view – 240 VA circuit keep-out area

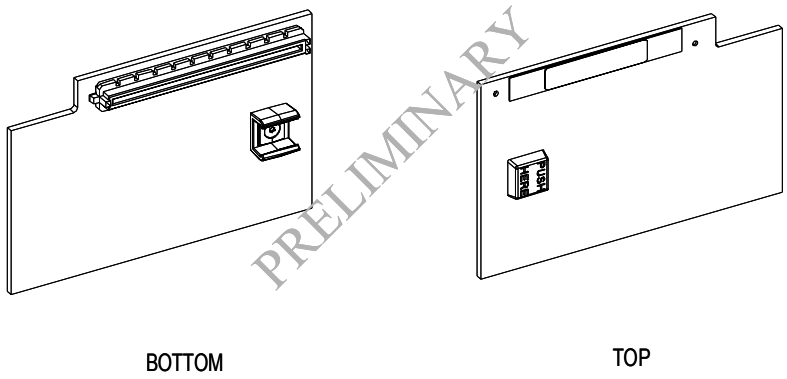


Figure 3.37. CIOv I/O Expansion Card (CIOv) – isometric views

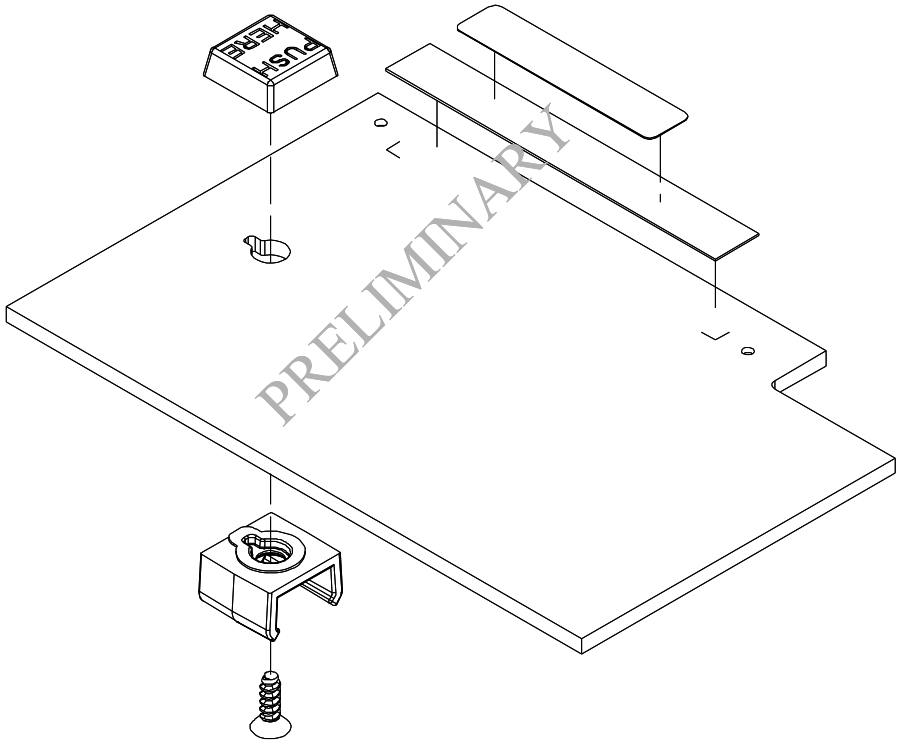


Figure 3.38. CIOv I/O Expansion Card (CIOv) – isometric view - exploded

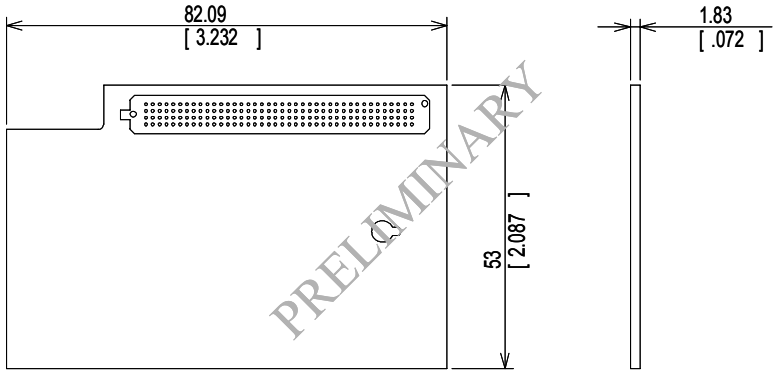


Figure 3.39. CIOv I/O Expansion Card (CIOv) – bottom and side view – card size, connector locations

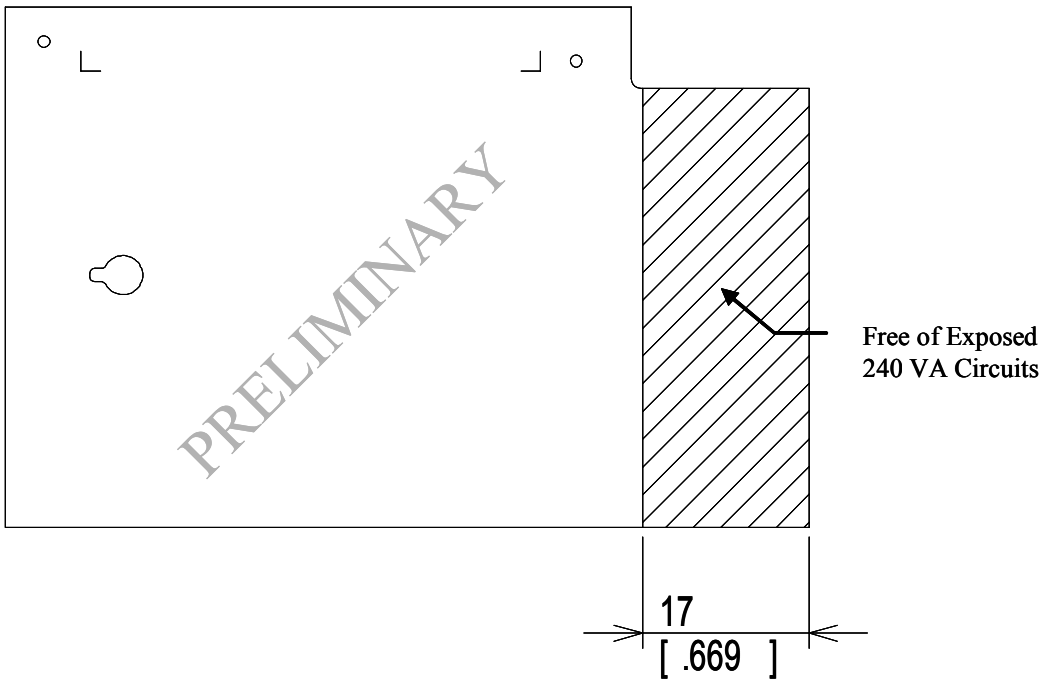


Figure 3.40. CIOv I/O Expansion Card (CIOv) – top view – 240 VA circuit keep-out area

4 Shock and Vibration

Shock and vibration test levels for blades, blade I/O expansion cards, and switch modules are defined in this section. Test levels for the BladeServer chassis are included for reference. It is recommended that tests at the blade, switch module, BladeServer chassis, and rack level be performed. However, in cases where this is not practical, blade and switch module testing using a rigid chassis test fixture as described below is, in most cases, acceptable.

Testing of the BladeServer chassis shall be performed at minimum and maximum chassis weight configurations. BladeServer: chassis testing shall be unpackaged, packaged, and in a rack. Testing of blades, blade I/O expansion cards, and switch modules shall be unpackaged, packaged, and in a chassis when practical (chassis unpackaged, packaged, and in a rack).

4.1 Pass/Fail Criteria

The product shall be inspected for mechanical damage after each test. Any noticeable damage is considered a failure. The product shall be operated before and after each test using an operating system and test exercise program to ensure it functions as designed.

4.2 Test Fixture

4.2.1 Operational Tests

For operational tests, the BladeServer chassis shall be clamped to the test table with rigid fixtures that support the chassis in a manner that simulates the support provided by the intended shipping package. Rack level operational vibration and shock testing is not performed.

4.2.2 Non-Operational Tests

For non-operational tests, the product shall be supported and clamped to the test table in a manner that simulates the support provided by the intended shipping package. For example, a blade should be mounted in a chassis which is clamped to the test table with rigid fixtures that support the BladeServer chassis as the shipping package does.

If a BladeServer chassis is not available, a rigid chassis test fixture for blades and switch modules may be used. This fixture shall be a rigid structure designed to simulate the support and retention mechanisms of the BladeServer. This structure should have a natural frequency of greater than 200 Hz. It shall provide the same guide channels, latch retention and connector system as a chassis. The signal and power connectors should be mounted on a board or other structure that will simulate the BladeServer midplane.

4.3 Operational Shock and Vibration

The following operational shock and vibration tests shall be performed on a test table. The tests are not performed in a rack.

4.3.1 Operational Shock

Server on, operational shock

- Vertical Input: 30.0 G for 3ms, half-sine shock pulse
- Horizontal Input: 15.0 G for 3ms, half-sine shock pulse
- Two shock inputs in each axis, one in each direction; six total

4.3.2 Operational Vibration

Server on, operational vibration: 0.27 G RMS at 5Hz to 500Hz for 30 minutes

Power Spectral Density (PSD) for operational vibration tests is provided in **Error! Reference source not found.**.

Table 4.1 - Random Vibration PSD Profile for Chassis, Blade and Switch Module Operational Unpackaged Test

Frequency	G^2 / Hz (PSD Level)
5.0	$2.0x10^{-5}$
17.0	$3.0x10^{-4}$
45.0	$3.0x10^{-4}$
48.0	$3.0x10^{-4}$
62.0	$3.0x10^{-4}$
65.0	$3.0x10^{-4}$
150.0	$3.0x10^{-4}$
200.0	$8.0x10^{-5}$
500.0	$8.0x10^{-5}$

4.4 Non-operational Shock and Vibration

Non-operational chassis, blade, blade I/O expansion card, and switch module vibration and shock test levels are defined below. Chassis level tests shall be performed with and without blades. In each case, the chassis shall be fully populated with modules. Chassis tests shall be performed using shock and vibration test tables and in a rack. Note that if blade level testing is performed in a BladeServer chassis, a maximum of 6 blades shall be tested at any one time. It is intended that blades, blade I/O expansion cards, and switch modules be tested as individual units and in the chassis. However, for companies developing blades, blade I/O expansion cards, and switch modules, an alternate test method is to use a rigid test fixture as described above, and test only to individual blade and switch module levels. This test method will result in a reasonable assurance that failure will not occur. However, if practical, it is recommended that chassis level testing be performed.

4.4.1 Non-operational Fragility Random Vibration

Unpackaged (fragility) random vibration tests are performed in accordance with levels in
. These levels are for the chassis, blades, blade I/O expansion cards, and switch modules. If the product fails during random vibration testing, additional sinusoidal vibration and dwell testing shall be used to determine weak areas of the product. The sinusoidal test shall consist of a sweep at 0.5G from 2Hz to 200Hz to determine the most dominant natural frequency then dwell at the natural frequency for 15 minutes. Once improvements are made to the design, the unpackaged random vibration tests shall be re-run to ensure compliance to the test levels.

Table 4.2 – Non-operational Unpackaged – Chassis, Blade, Blade I/O Expansion Card, and Switch Module

Orientation	GRMS	Duration (minutes)
Bottom	1.463	15
Top	1.463	15
Right	1.463	15
Left	1.463	15
Front	1.463	15
Rear	1.463	15

The random vibration test spectrum for non-operational unpackaged testing shall be in accordance withTable 4.3.

Table 4.2 - 1.463 GRMS Random Vibration Spectrum for Chassis, Blades, and Switch Module Tests

Frequency	G^2 / Hz (PSD Level)
2.0	0.0010
4.0	0.0300
8.0	0.0300
40.0	0.0100
200.0	0.0100

4.4.2 Non-operational Fragility Shock - Unpackaged Chassis

Table 4.4defines the unpackaged chassis shock test levels. BladeServer does not pass an unpackaged 35 G rear drop at a change in velocity of 3.459 mm/s with 14 blades. Therefore, for blade testing, no more than 6 blades shall be tested in an unpackaged chassis at any one time.

Table 4.3 - Non-Operational Unpackaged Fragility Chassis Shock Test Levels

Orientation	G's	Delta-V mm/sec (in./sec)	Wave Form
Bottom	35	3,459 (136.19)	Trapezoid
Top	35	3,459 (136.19)	Trapezoid
Right	35	3,459 (136.19)	Trapezoid
Left	35	3,459 (136.19)	Trapezoid
Front	35	3,459 (136.19)	Trapezoid
Rear	35	3,459 (136.19)	Trapezoid

4.4.3 Non-operational Fragility Shock – Unpackaged Blade and Switch Module

Unpackaged blade and Switch module shock test levels are defined in Table 4.5.
Blades and switch modules may be qualified using a rigid chassis test fixture, as described in the test fixture section of this document, in lieu of the chassis level test described in the section above. The levels in Table 4.5 shall be used to test blades and switch modules in the rigid chassis test fixture.

Table 4.4 - Non-Operational Unpackaged Blade and Switch Module Shock Test Levels

Orientation	G's	Delta-V mm/sec (in./sec)	Wave Form
Bottom	50	4,572 (180)	Trapezoid
Top	50	4,572 (180)	Trapezoid
Right	50	4,572 (180)	Trapezoid
Left	50	4,572 (180)	Trapezoid
Front	50	4,572 (180)	Trapezoid
Rear	50	4,572 (180)	Trapezoid

4.4.4 Non-operational Packaged Random Vibration

Packaged random vibration tests are performed in accordance with levels in Table 4.5. These levels are for the chassis, blades, blade I/O expansion cards, and switch modules.

Table 4.5 - Non-operational Packaged - Chassis, Blade, Blade I/O Expansion Card, and Switch Module

Orientation	GRMS	Duration (minutes)
Top or Bottom	1.463	15
Right or Left	1.463	15
Front or Rear	1.463	15

The random vibration test spectrum for non-operational unpackaged testing shall be in accordance with Table 4.3

4.4.5 Non-operational Packaged Shock – BladeServer Chassis

Table 4.5lists the chassis packaged drop test levels. Product acceleration response inside the package must be monitored during the test. The response must be lower than the unpackaged fragility acceleration target.

Table 4.6 - Non-operational Packaged Chassis Drop Test Levels

Orientation	Drop Height mm (inches)
Bottom	610 (24)
Top	610 (24)
Right	610 (24)
Left	610 (24)
Front	610 (24)
Rear	610 (24)

4.4.6 Non-operational Shock – Packaged Blade, I/O Expansion Card and Switch Module

Table 4.7 lists the drop heights for specific weight ranges to be used to test packaged blade, I/O expansion cards, and switch modules. Product acceleration response inside the package must be monitored during the test. The response must be lower than the unpackaged fragility acceleration target.

Table 4.7 - Non-operational Packaged Blade, Blade I/O Expansion Card and Switch Module Drop Test Levels

Orientation	Drop Height mm (inches) Weight < 9.1 Kg (20 lbs)	Drop Height mm (inches) Weight = 9.1 Kg (20 lbs) to 18.2 Kg (40 lbs)	Drop Height mm (inches) Weight = 18.2 Kg (40 lbs) to 36.4 Kg (80 lbs)
Bottom	914 (36)	762 (30)	610 (24)
Top	914 (36)	762 (30)	610 (24)
Right	914 (36)	762 (30)	610 (24)
Left	914 (36)	762 (30)	610 (24)
Front	914 (36)	762 (30)	610 (24)
Rear	914 (36)	762 (30)	610 (24)
Critical Corner	914 (36)	762 (30)	610 (24)
Critical Edge	914 (36)	762 (30)	610 (24)

4.4.7 Non-operational Shock – Chassis, Blades, I/O Expansion Cards and Switch Modules Installed in a Rack

Table 4.8 lists the non-operational rack shock test levels for a chassis with blades and switch modules installed.

Table 4.8 - Non-operational Rack Shock Test Levels for Chassis with Blades and Switch Modules Installed

Drop Height mm (in.)	Wave Form	Duration	Target Delta V mm/sec (in./sec)	# of Drops	Drop Description
152.4 (6)	Half Sin	< 3 ms	1,730 (68.09)	2	Bottom Face (Shipping Orientation)
50.8 (2)	Half Sin	< 3 ms	998.5 (39.31)	10	Bottom Face (Shipping Orientation)

4.4.8 Non-operational Random Vibration - Rack

Random rack vibration tests shall be tested to the levels described below. If the product fails during random vibration testing, additional sinusoidal vibration and dwell testing shall be used to determine weak areas of the product. The sinusoidal test shall consist of a sweep at 0.5G from 2Hz to 200Hz to determine the most dominate natural frequency then dwell at the natural frequency for 15 minutes. Once improvements are made to the design, the unpackaged random vibration tests shall be re-run to ensure compliance to the test levels.

Table 4.9 - Non-operational Unpackaged – Rack Testing with Chassis, Blade, Blade I/O Expansion Card, and Switch Modules

Orientation	GRMS	Duration (minutes)
Bottom	1.04	15

The random vibration test spectrum for non-operational rack testing shall be in accordance with Table 4.10.

Table 4.10 - 1.04 GRMS Random Vibration Spectrum for Rack Tests

Frequency	G^2 / Hz (PSD Level)
2.0	0.0010
4.0	0.0300
8.0	0.0300
40.0	0.0030
55.0	0.0100
70.0	0.0100
200.0	0.0010

4.5 Telco Environment

For Telco environment, abide by Telcordia GR-63-CORE.