SmartNICs and SmartSSDs, the Future of Smart Acceleration

Scott Schweitzer
Xilinx
Abstract

Since the advent of the Smart Phone over a decade ago, we've seen several new "Smart" technologies, but few have had a significant impact on the data center until now. SmartNICs and SmartSSDs will change the landscape of the data center, but what comes next? This talk will summarize the state of the SmartNIC market by classifying and discussing the technologies behind the leading products in the space. Then it will dive into the emerging technology of SmartSSDs and how they will change the face of storage and solutions. Finally, we'll dive headfirst into the impact of PCIe 5 and Compute Express Link (CXL) on the future of Smart Acceleration on solution delivery.
Agenda

- Framing
- SmartNICs
- SmartSSDs and Computational Storage
- Rise of the Accelerators
Framing – Accelerators Aren’t New

- Mainframes had them in the 1950s
- Expensive Tube-base IBM 709
- Intelligent I/O Controller IBM 7607
Framing – Server Issues

- CPUs scale-out versus scale-up
- GPUs validated need
- SDE: Programmability, composability & orchestration
Framing – Speeds

- Net, GbE till 2010, 10Gb, 25Gb, soon 100Gb
- Disks in ms, SSD us
- CPU densities soar
Framing – Corporate Players

NVIDIA $300B
  Mellanox
  Cumulus Networks
  ARM

Intel $210B

AMD $90B

Samsung $330B

Marvell $26B

Xilinx $24B

TI $125B

Qualcomm $127B

Broadcom $144B
SmartNICs, What’s the big deal?
SmartNICs: Why?

- SmartNICs: Networking = GPUs: HPC
- Arrived later, wider market
- Separate domain, security & orchestration
- CPU power rivals x86
- Benefits from new PCIe & protocols
SmartNICs: Who?

- Financials
- Hyper-scalers
- Streamers
- SmartWorld Applications
SmartNICs: Architecture

**Management Plane**
Tools for managing the Network
CLI, REST API, SNMP

**Control Plane**
Signaling between network entities exchanging state
Distributed (OSPF & BGP), Centralized (OpenFlow, OVSDB)

**Data Plane**
Data path for network packets
P4, IPTables, OVS, DPDK, BPF, Routing Tables

*Note Borrowed from: [Docker Networking: Control Plane Data Plane Presentation](https://example.com)*
SmartNICs: Building Blocks

- **Hardware**
  - Cores, IP, Programable Logic, Memory & Interconnect

- **Protocols**
  - PCIe, CXL, CCIX, Ethernet, IB, UDP, TCP, HTML/3 & QUIC

- **Ecosystem**
  - Languages, SDK & App Stores
SmartNICs Top Six: Stingray/Broadcom

- ASIC Based
  - Flow classifier
  - 8 ARM Cores
  - IP Accelerators
- Memory
  - 2 Banks DDR4
SmartNICs Top Six: Fungible

- ASIC Based
  - MIPS64
- IP Accelerators
- Memory
  - 2 Banks DDR4
- HBM
SmartNICs Top Six: Vista Creek/N3000/Intel

- Complex Multi-chip (7)
  - ASIC
    - 2x XL710
    - Max10
    - 2x C827
    - PEX8747
  - FPGA
  - Memory 2x DDR4
SmartNICs Top Six: BlueField2/NVIDIA

- ASIC Based
  - ConnectX-6 Dx
  - 8 ARM Cores
  - IP Accelerators
- Memory
- DDR4
SmartNICs Top Six: Naples/Pensando

- ASIC Based
  - P4 Engine
  - 8 ARM Cores
  - IP Accelerators
- Memory
SmartNICs Top Six: U25/Xilinx

- ASIC – X2
- FPGA – Zynq
  - Large FPGA
  - 4 ARM Cores
- Memory
  - 2x DDR4
SmartNICs: Evolving Issues

- Separate Computational Domain
- P4 and PNA
- Cores and Planes
- Protocols
- Security
- Orchestration
SmartSSDs & Computational Storage
FPGAs in Storage Today

- Flash controllers

- Storage Systems
  - Cache-offload
  - Storage System & Switching connectivity
  - Data Reduction
FPGA Advantages for Computational Storage

- Flexible, fully customizable architecture adapts to specific applications
  - Massive parallelism, I/O and customizable data path
- Performance, power and latency of dedicated HW + reconfigurability of SW
- More economical than ASIC/ASSP for many applications
FPGA Advantages for Changing Standards

Architecture easily adapts to latest compression algorithms
Computational Storage Drive (CSD)

- Integrated Accelerator and Flash

Benefits:
- Easy to implement - plug & play
- Adding capacity adds accelerators + performance
- Ability to optimize BW between accelerator and flash
- Ability to customize FTL for specific workloads

Xilinx Partners:
- Samsung
- Scaleflux
Computational Storage Processor (CSP)

Accelerator and Storage on same PCIe subsystem

Benefits:
- Independent SSD & acceleration scaling
- Plugs into standard slot
- PCIe Peer-to-peer transfers for high bandwidth and low latency

Xilinx Partners:
- Bittware
- Eideticom
- Xilinx
Computational Storage Array (CSA)

Accelerator in-line with storage

Benefits:
- SSD vendor independence
- Independently scale accelerators and SSDs
- Ability to optimize BW between accelerator and SSDs

Xilinx partners:
- Bittware
Rise of the Accelerators
Rise of Accelerators - Protocols

- PCIe Gen5
- PCIe Peer to Peer
- CXL
- CCIX
Rise of Accelerators – PCIe Gen5

- Brings the expected 2X speed bump
- Support for PCIe Peer to Peer
- New protocols (CXL & CCIX)
Rise of Accelerators – PCIe Peer to Peer (P2P)

- 2018 Linux kernel finally added support
  - Previously needed to control both ends
- Ideal for Accelerator to NVMe
- No support beyond two accelerators
Rise of Accelerators - CXL

- Compute eXpress Link (CXL)
- Master-Slave model with Cache Coherence
  - CPU cache
  - Main memory
  - Accelerator memory
Rise of Accelerators - CCIX

- Cache Coherent Interconnect for Accelerators (CCIX)
- Peer to Peer model
- Non-Uniform Memory Access (NUMA) mapping
  - Host and multiple devices single virtual addressing
Rise of Accelerators – Security

- Separate Compute Domain
- Kernel Transport Link Security (kTLS)
- Confidential Computing Consortium (CCC)
- Orchestration
- Xilinx Manager
Rise of Accelerators – Use Case SmartWorld

- Three major applications
  - Video Decode
  - AI/ML Locate
  - Transcode
- Real-Time Requirement
More Resources by the Speaker

- **Electronic Design – SmartNIC Series**
  - What Makes a SmartNIC Smart?
  - Why is a SmartNIC Better Than a Regular NIC?
  - SmartNIC Architectures: A Shift to Accelerators and Why FPGAs are Poised to Dominate
  - How PCIe 5 with CXL, CCIX, and SmartNICs Will Change Solution Acceleration

- **IEEE Hot Interconnects 2020 – SmartNIC Panel**
Thank You for Attending

Please take a moment to rate this session.

Your feedback matters to us.