

Storage Developer Conference September 22-23, 2020

# Smart Storage Adapter for Composable Architectures

Rémy GAUGUEY Sr Software Architect



# Kalray at SDC20

Kalray is well represented this year at SDC with 4 sessions! Please have a look.

- A NVMe-oF Storage Diode for Classified Data Storage Jean-Baptiste Riaux, Sr Field Application Engineer
- High-performance RoCE/TCP Solutions for End-to-end NVMe-oF Communication Jean-François Marie, Chief Solution Architect
- Next Generation Datacenters Require Composable Architecture Enablers and Programmable Intelligence Jean-François Marie, Chief Solution Architect
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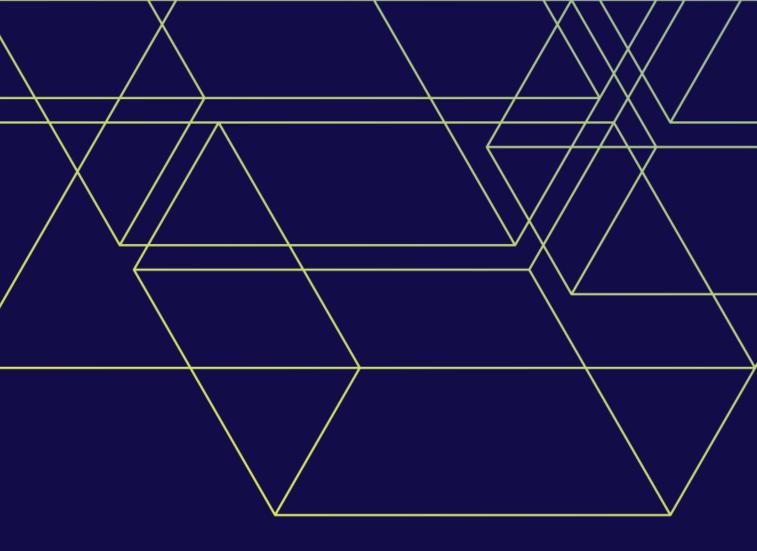
 Smart Storage Adapter for Composable Architectures Rémy Gauguey, Sr Software Architect











# Abstract

# **Smart Storage Adapter for Composable Architectures**

The variety of architectures, use-cases and workloads to be managed by Data Center appliances is increasing. It is driving a need for storage and compute disaggregation, while at the same time forcing IT pros to simplify Data Center management and move to hyperconverged infrastructure. However the HCI approach results in siloing of storage that leads to capacity waste and scalability issue.

This paper describes how Kalray's fully programmable Smart Storage adapter leverages NVMe-oF technology to offload servers from heavy storage disaggregation task, and pave the way toward a fully Composable Infrastructure.





# The Presenter

# **About the Presenter**



**Rémy Gauguey** is a Senior Software Architect at Kalray, for the Data Center Business Unit. He has more than 25 years of experience in the high tech industry, with strong expertise in SoCs, RTOS and high performance packet processing.

He develops advanced architectures for composable infrastructure, leveraging the MPPA® manycore technology from Kalray.

Rémy has been previously developing his expertise at Conexant, Mindspeed Technologies and the CEA labs. He holds several patents in the fields of software architecture and packet processing.





# Smart Storage Adapter for Composable Architectures

# THE DATA PROCESSING UNIT REVOLUTION In the Data-Centric Era

### Scale-out data center & micro-services based applications



**Network traffic explosion** East-West traffic, multi-tenant, overlays...



**Data Storage Capacity explosion** Storage spread across servers / disaggregation

Multi-tenant and **security** threat Cryptography everywhere (storage, network...)



1

More and more **complex** data processing Al, analytics ...



computation Storage stack, network stack, crypto...



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### **General purpose CPU and OS** inefficiencies

# ~25% of the servers **power** spent in data centric

# **General Purpose CPUs** inefficient for



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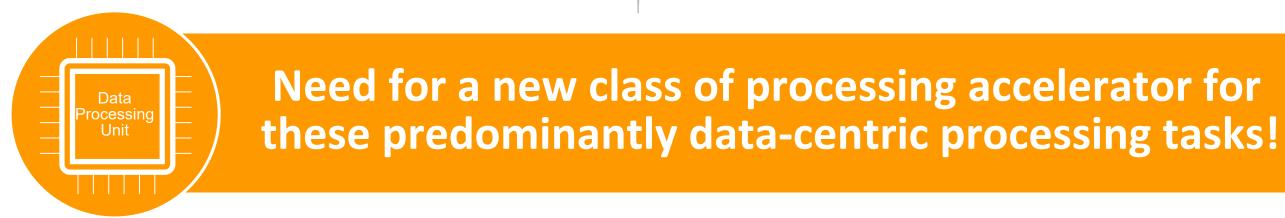


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<b>1 HCI</b> (Hyper Converged Infrastructure)	2 Disaggregation	
<ul> <li>Reduce complexity and hardware sprawl</li> </ul>	<ul> <li>Larger and larger datasets generated by</li> </ul>	•
Reduce costs	Containerized applications and VMs	
<ul> <li>Increase agility and scalability</li> </ul>	<ul> <li>Large diversity of application workloads</li> </ul>	

# 3 Composable



<b>1 HCI</b> (Hyper Converged Infrastructure)	Oisaggregation	
<ul> <li>Reduce complexity and hardware sprawl</li> <li>Reduce costs</li> <li>Increase agility and scalability</li> </ul>	<ul> <li>Larger and larger datasets generated by Containerized applications and VMs</li> <li>Large diversity of application workloads</li> </ul>	• /

### **HCI** 2.0 architecture is a solution for HCI/Disaggregation ...

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# 3 Composable



<b>1 HCI</b> (Hyper Converged Infrastructure)	2 Disaggregation	
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### **HCI** 2.0 architecture is a solution for HCI/Disaggregation ...



- Additional load on HCI cluster CPU by SW disaggregation
- Additional load on HCI cluster interconnect
- Storage Disaggregation is complex and expensive
- Clusters scalability limitation

#### HCI does not enable COMPOSABILITY

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# 3 Composable



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#### HCI does not enable COMPOSABILITY



# Need a new approach for a truly COMPOSABLE infrastructure!

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### 3 Composable



#### CPU CPU CPU core core core

No new services / no possible evolution!

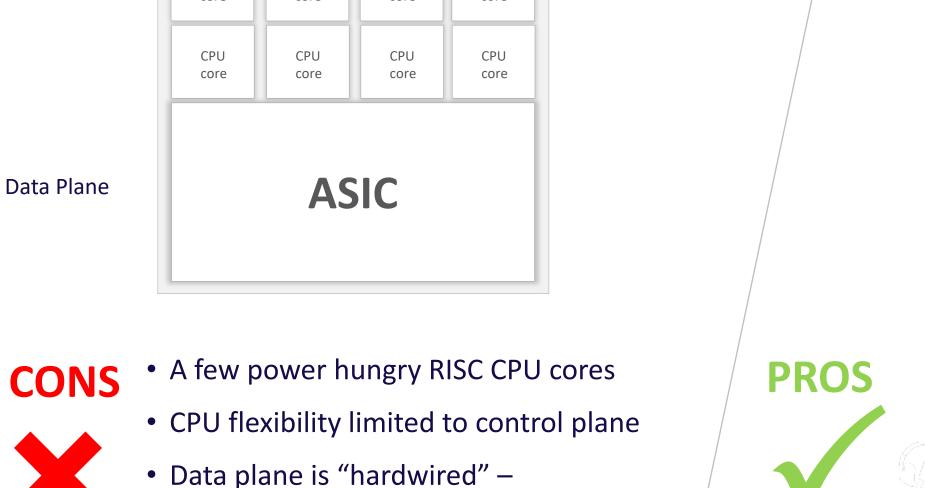
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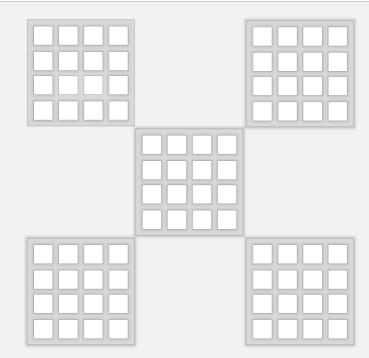
# "SmartNic" Usual Approach

CPU

core

**Control Plane** 





**Power efficiency** 25W Typ

**High Speed I/O** 2x100Gbps,PCIGen4,DDR4

# COOLIDGE™: THE ULTIMATE I/O PROCESSOR Why Coolidge is a Revolution vs Competition?

# Kalray's MPPA<sup>®</sup>3 Coolidge<sup>™</sup>

**80** highly efficient VLIW independent **CPU** cores, gathered into 5 clusters, running at **1.2GHz**, connected to high speed fabrics & high speed interfaces.

### </> Fully programmable

Control Plane / Mgt Plane – Linux – 16 cores Data Plane - 64 cores



#### **Top Performance**

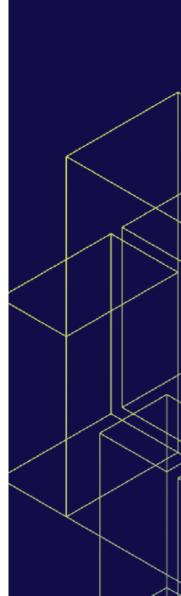
**Any workload** 

200KDMIPs, 25TOPS

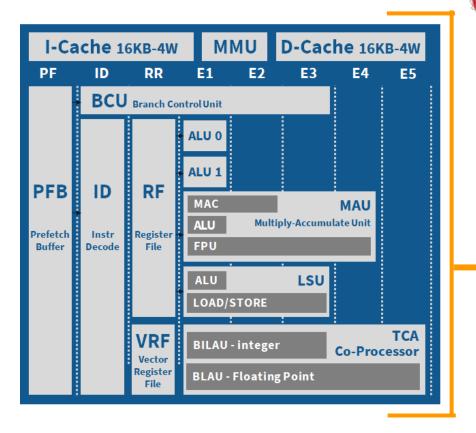
**Functional Isolation & Safety** 

Secure Islands, Encrypt/Decrypt, Secure Boot



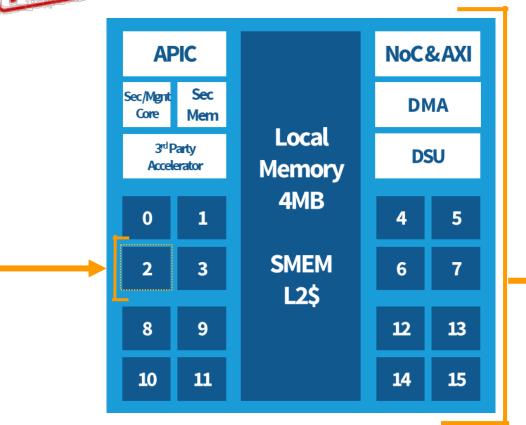


# MPPA® COOLIDGE ARCHITECTURE The I/O Processor for Next Gen Intelligent Systems



#### **3<sup>RD</sup> GENERATION KALRAY CORE**

- •VLIW 64-bit core
- •6-issue VLIW architecture
- •MMU + I&D cache (16KB+16KB)
- •16-bit/32-bit/64-bit IEEE 754-2008 FPU
- •Vision/CNN Co-processor (TCA)



#### **CLUSTER**

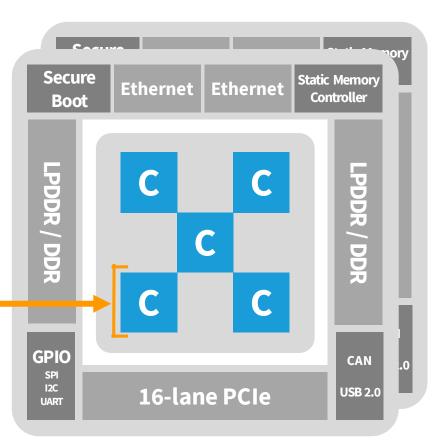
#### Architecture

- 16 cores
- 1 safety/security dedicated core
- 600 to 1200 MHz

#### Memory

- L1 cache coherency (configurable)
- 4MB configurable memory (L2 cache)
- 256 bits / bandwidth up to 614GB/s)

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#### **MULTI CLUSTER ARCHITECTURE**

#### 5 Clusters: 80 cores + 80 co-processors

- •Load Balancer / Packet Parser
- •2x100Gbps Ethernet
- PCIGen4
- •DDR4 3200

#### AXI Bus + NoC Bus

- •L2 refill in DDR and direct access to DDR from clusters
- •DMA-based highly efficient data connection



# DATA CENTRIC COMPUTATION Workloads and Requirements

DATA CENTRIC WORKLOAD CHARACTERISTICS	DATA PROCESSING UNIT REQUIREMENTS
High parallelism Many stateless or stateful contexts : TCP/IP, TLS, IPsec sessions , NVMe queues	Manycore (MIMD) architecture
Short temporal data locality Complex memory hierarchy L1/L2/L3 not well suited	Large on chip memory (TCM) - With large bandwidth - Simple and deterministic memory subsystem
<b>I/O intensive</b> High IOPS and GB/s, low latency	<ul> <li>Optimized interconnect         High bandwidth, low latency &amp; deterministic on chip     </li> <li>High speed interfaces</li> </ul>
<b>Computational intensive</b> Inline AI inference, analytics, crypto, erasure coding	<ul> <li>Floating Point Unit</li> <li>Al acceleration</li> <li>Cryptographic acceleration</li> <li>Erasure Coding acceleration</li> </ul>
Variability and flexibility Programmability / flexibility (C, C++, standard APIs)	- C / C++ programmable data plane - Standard APIs





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# SD20 G KALRAY

C KALRAY

HEOBGA 1156V100

MANYCORE

#### KALRAY'S MPPA®3 COOLIDGE™

- 80 VLIW cores @ 1.2 GHz
- 5 Clusters x16 cores



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#### C KALRAY KALRAY'S MPPA®3 COOLIDGE<sup>™</sup>

- 80 VLIW cores @ 1.2 GHz
- 5 Clusters x16 cores
- - 20 MBTCM
  - 5 isolated clusters with \$L2



MANYCORE

HECOGA 1156V10

DATA CENTRIC WORKLOAD CHARACTERISTICS	DATA PROCESSING UNIT REQUIREMENTS
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  - 2x100 Gbps Ethernet
  - PCle x16 Gen4 (RC/EP)



C KALRAY

HEORGA 1156V100

MANYCORE

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  - Up to 1.15 TFLOPs (SP)
  - Up to 25 TOPs (8bits)/4.2TFLOPS (HP) for AI
  - 100 Gbps + Crypto acc.
  - Line rate Reed Solomon



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- 100 Gbps + Crypto acc.
- Line rate Reed Solomon
- Linux, OpenDataPlane
- SPDK BDEVs, NVMe
- OpenCL

# 

C KALRAY

MANYCOR

# Kalray Smart Storage Adapter Solutions

# $MPPA^{(R)}$

The Processor at the Heart of Intelligent Systems





# KALRAY SMART STORAGE ADAPTER SOLUTION K200 / K200-LP & ACS SDK

### K200 & K200-LP

manufactured by wistron

#### **2** Form Factors

- FHHL (Full Height) K200 Single Slot
- HHHL (Low Profile) K200-LP Single or Double Slots

#### **Manycore Architecture**

- 80 VLIW cores @ 1.2 Ghz
- 5 Clusters x16 cores

#### **High Speed Ethernet**

- 2x100GbE / 8x25 GbE

#### **Certified NVMe-oF Stack**

- NVMe-oF 1.1 (Target, Intiator)
- RoCE v1/v2, TCP

#### **Advanced SSD interface**

- PCIe-Gen4
- NVMe 1.1 to 1.4 SSDs No need for CMB
- Dual port SSD support

#### 2 Modes

- Stand-alone
- Host CPU co-processor
- / "host-agnostic" support

#### **Agnostic Host Support**

- NVMe Driver

#### **DDR-3200**

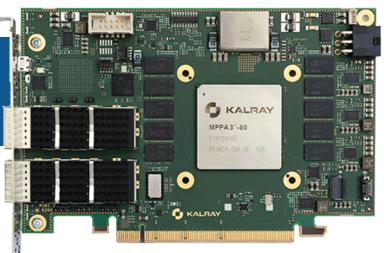
- 8GB to 32GB

#### **H/W Accelerators**

- Encryption / Decryption
- Hashing (SHA-256, SHA-3)
- Erasure Coding

#### **Low Power**

- 35W (single slot)
- 65W (double slot)



K200 Smart Adapter

#### Key figures (per card)

- Random R/W RoCE: 4-6 MIOPS
- Random R/W TCP: 2-4 MIOPS
- Sequential R/W (RoCE&TCP):
   25GB/s
- Latency (RoCE/TCP): 10 /30 usec

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AccessCore® Open Software & Tools

#### **Open Software Environment**

- Linux / SPDK Control Plane (16 Cores)
- Fully Programmable Data Plane (64 Cores)
- Storage, Network and Compute Services (AI,DSP,NVMe,NVMe-oF,ROCE,TCP, RAID, de-dup,...)

#### **Agnostic Host Support**

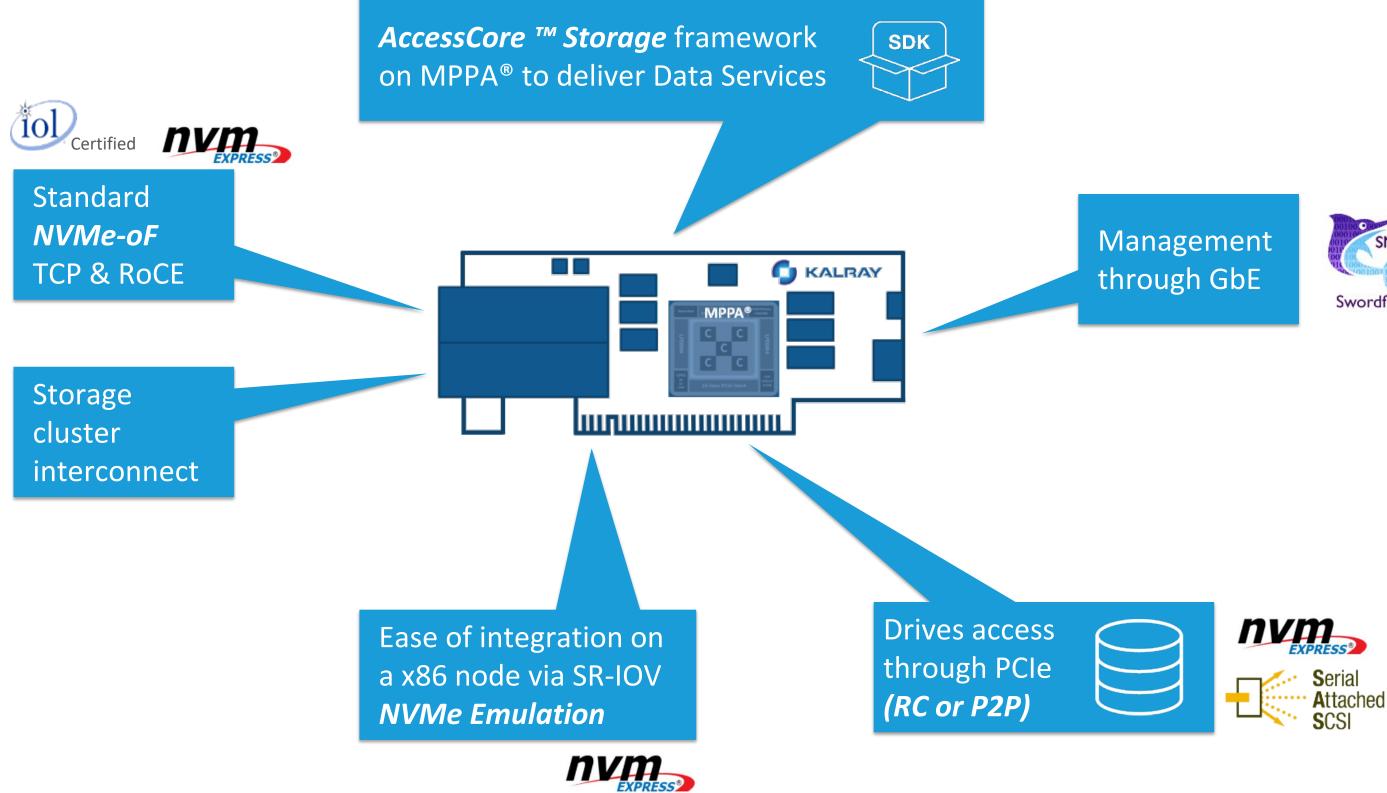
- NVMe Driver

#### + Extra compute available

- @ 3MIOPS, 50% cores available !
- Storage Services (RAID, de-dedup ...)
- Al
- Analytics ...



# **KALRAY SMART STORAGE ADAPTER SOLUTION** Simplified Integration into any System

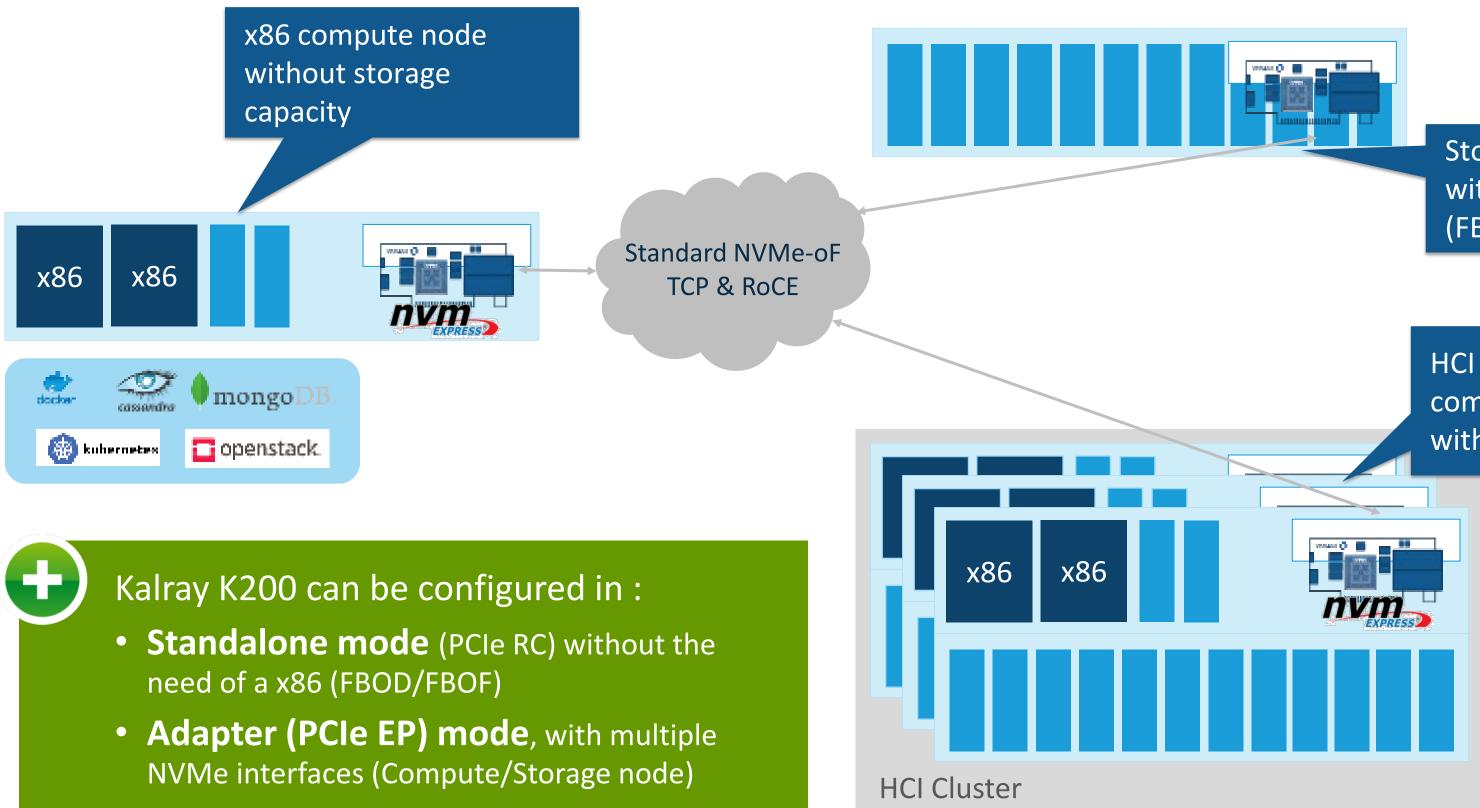








# **KALRAY SMART STORAGE ADAPTER** Where Does It Fit?



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Storage shelf with PCIe slots (FBOD/FBOF)

HCI x86 storage or compute node with capacity

SD<sub>20</sub> 

# EXAMPLE: LYMMA JBOF REFERENCE PLATFORM White Label NVMe-oF (RoCE/TCP) JBOF

### Hyper Optimized JBOF (no x86)

- JBOF Chassis:
  - Stand-alone
  - 2U 1200W Redundant
  - 24 U.2 NVMe SSDs
  - 6xPCle Gen3 x16
- Kalray Smart Controller Cards
  - 2 to 6 Cards
- BMC chip AST2500 (ASpeed)
- 1Gbps management interface



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NVMe SSDs

**Redundant Power** 

System Cooling FANs

PCIe Card Cages 12







# Kalray AccessCore® Storage (ACS) Framework

# $MPPA^{(R)}$

The Processor at the Heart of Intelligent Systems







# ACCESSCORE FOR STORAGE & NETWORKING ACS4.x Architecture Highlights

### PROGRAMMABILITY

- Full programmability on data, control & management planes
  - Control & Management plane : Linux (typical : 1 Cluster - 16 cores)
  - Data plane : Cluster OS (light POSIX OS)
     (typical: 1 to 4 Clusters 16 to 64 cores)



- Run to completion full dataplane
  - From network functions to NVMe stack on light OS cores
- True inline processing
  - No need for x86 pre/post processing

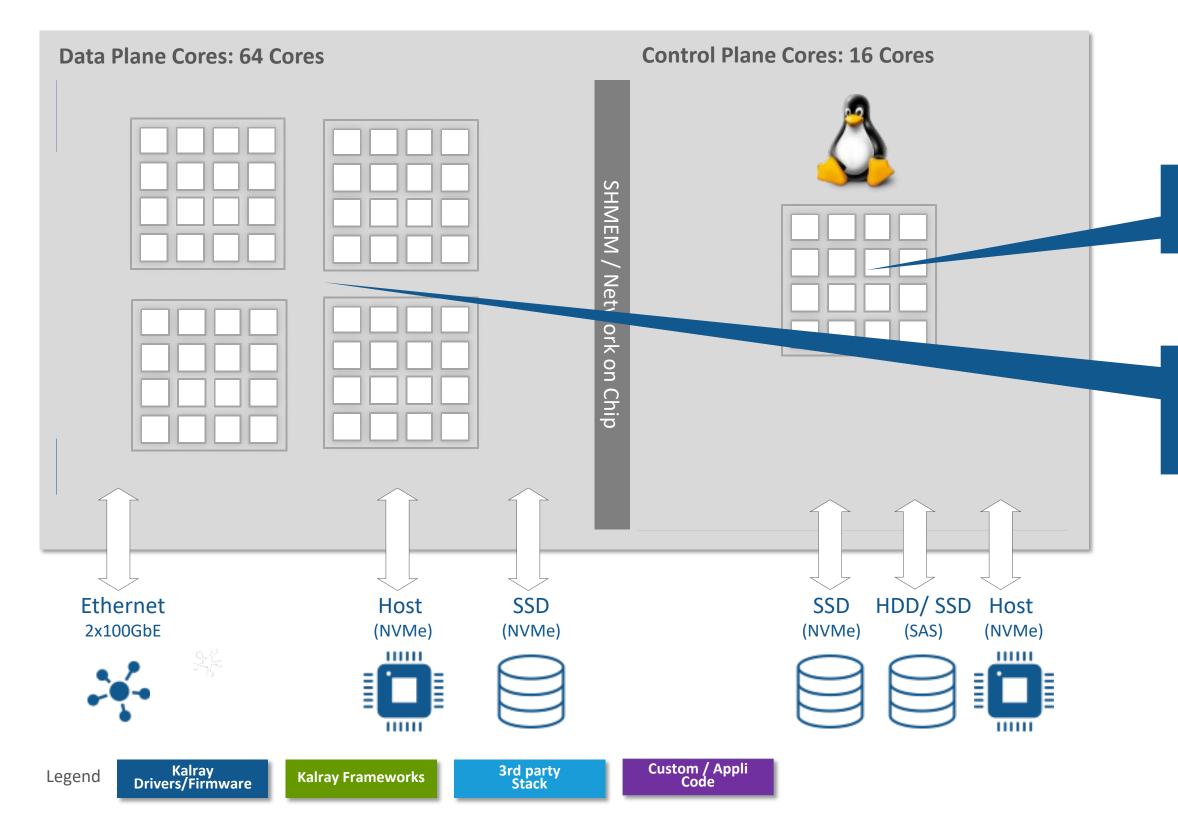
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# **STANDARDIZED**

- Hardware interfaces
  - NVMe emulation
- Software APIs & tool chain
  - Linux APIs: SPDK, virtio, ibverbs ...
  - Data plane APIs: sockets, SPDK nvme lib, SPDK BDEV, ODP
  - Librairies : ISA-L, Buildroot, binutils







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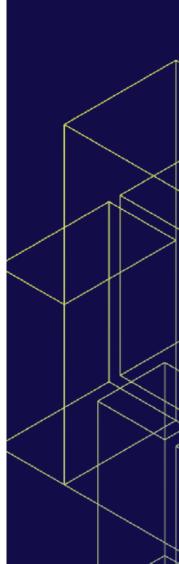




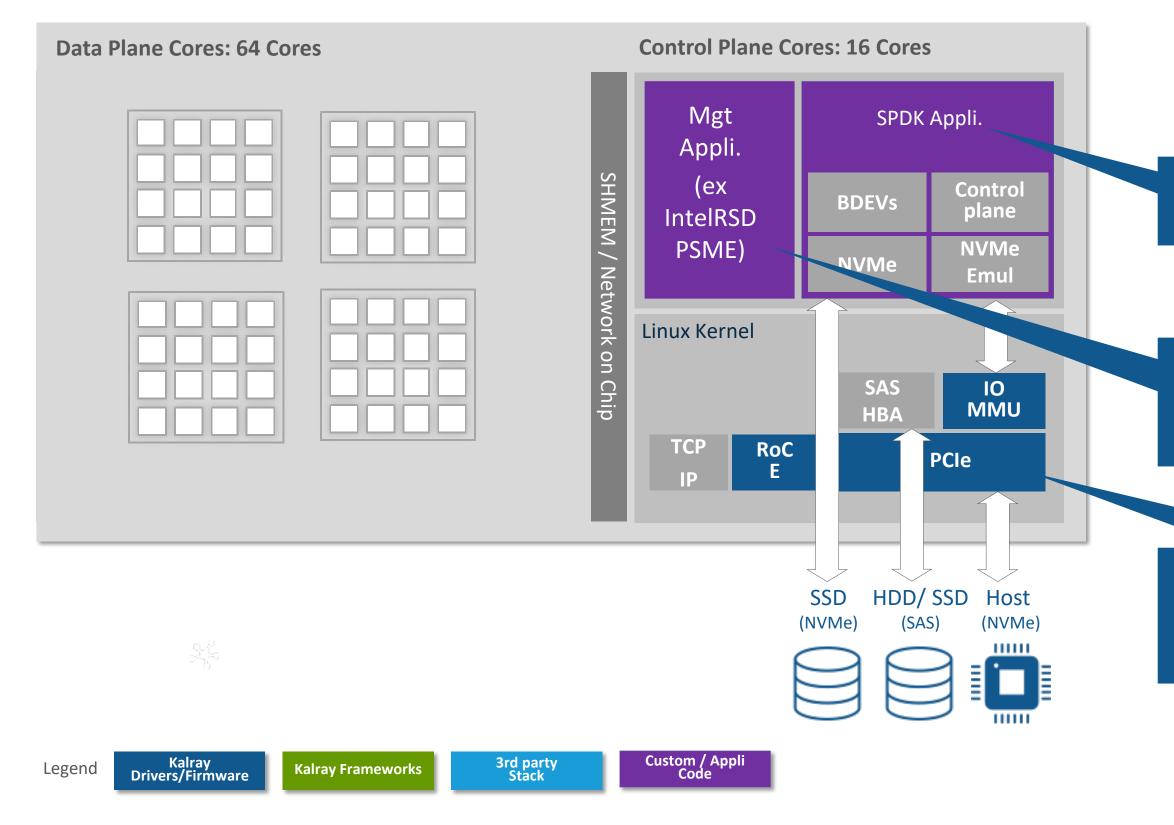


*Linux* on control plane cluster (16 cores)

ClusterOS on 4 data plane clusters (64 cores)







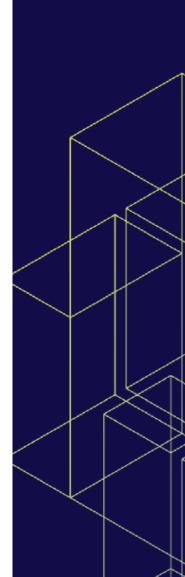
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SPDK on Linux user space for control plane ONLY

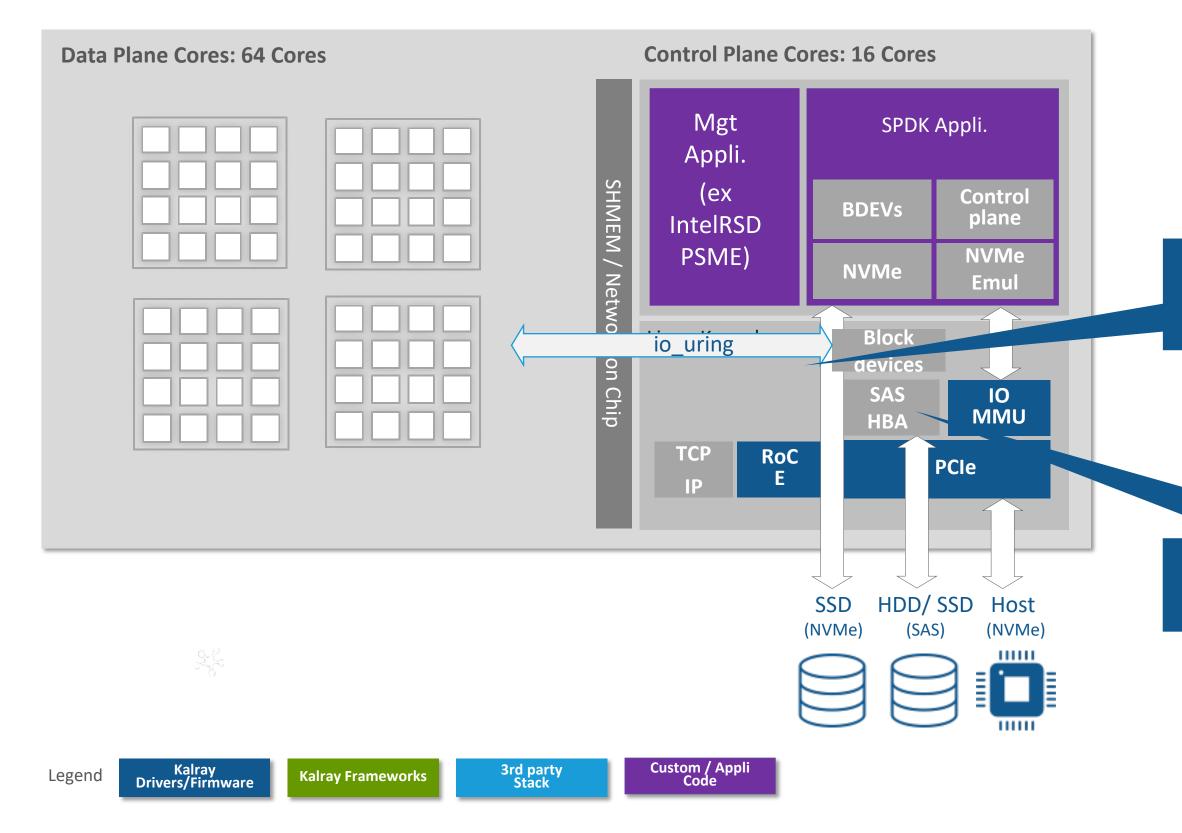
Redfish/Swordfish support via IntelRSD

PCIe P2P : PCIe RC emulation to control x86 attached devices (NVMe, SAS HBA)









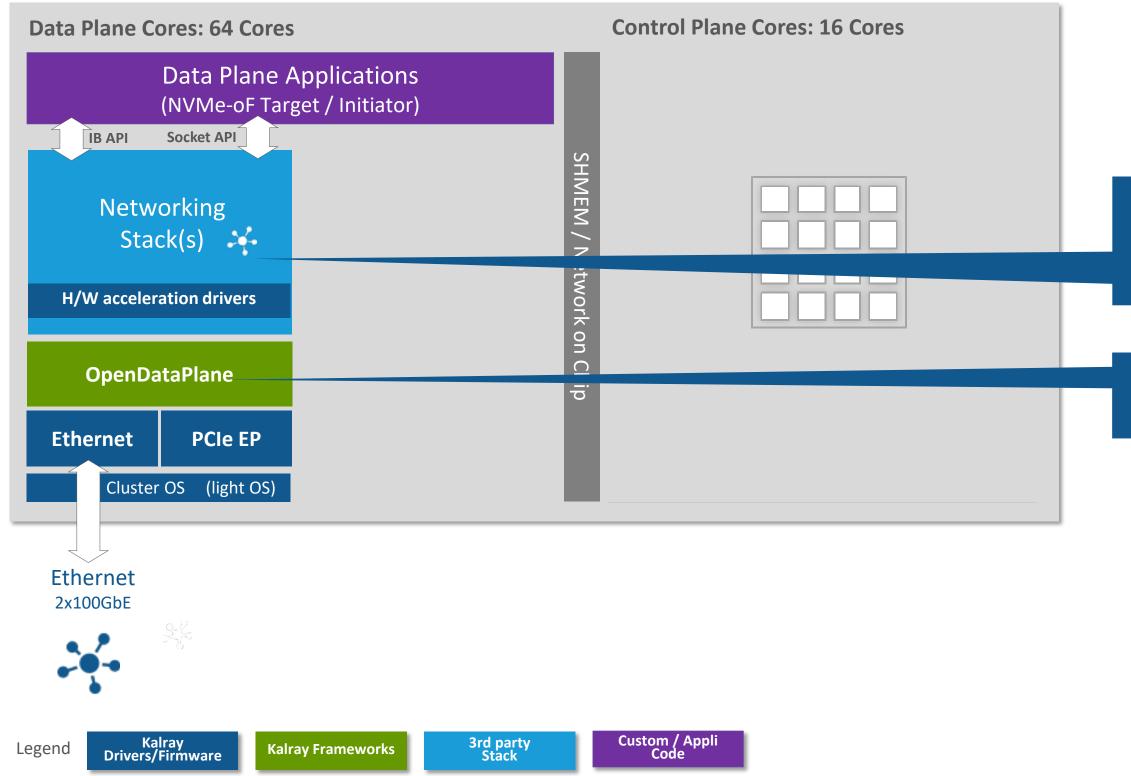
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ONLY for SAS : Data plane comm. using io\_uring (1MIOPs @4K)

SAS HBA driver for external add in card







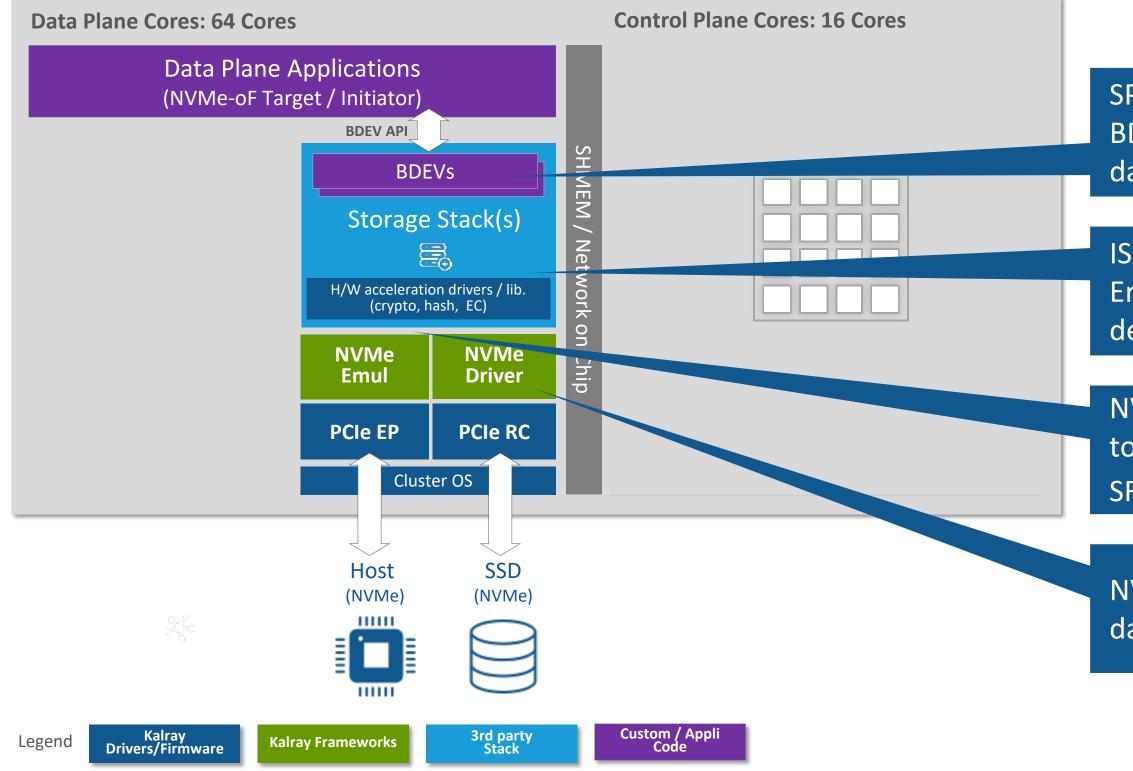
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3<sup>rd</sup> party optimized network stack (TCP/IP, RoCE)

OpenDataPlane







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SPDK on Cluster OS BDEVs porting over data plane

ISA-L compliant lib for Erasure Coding, deflate

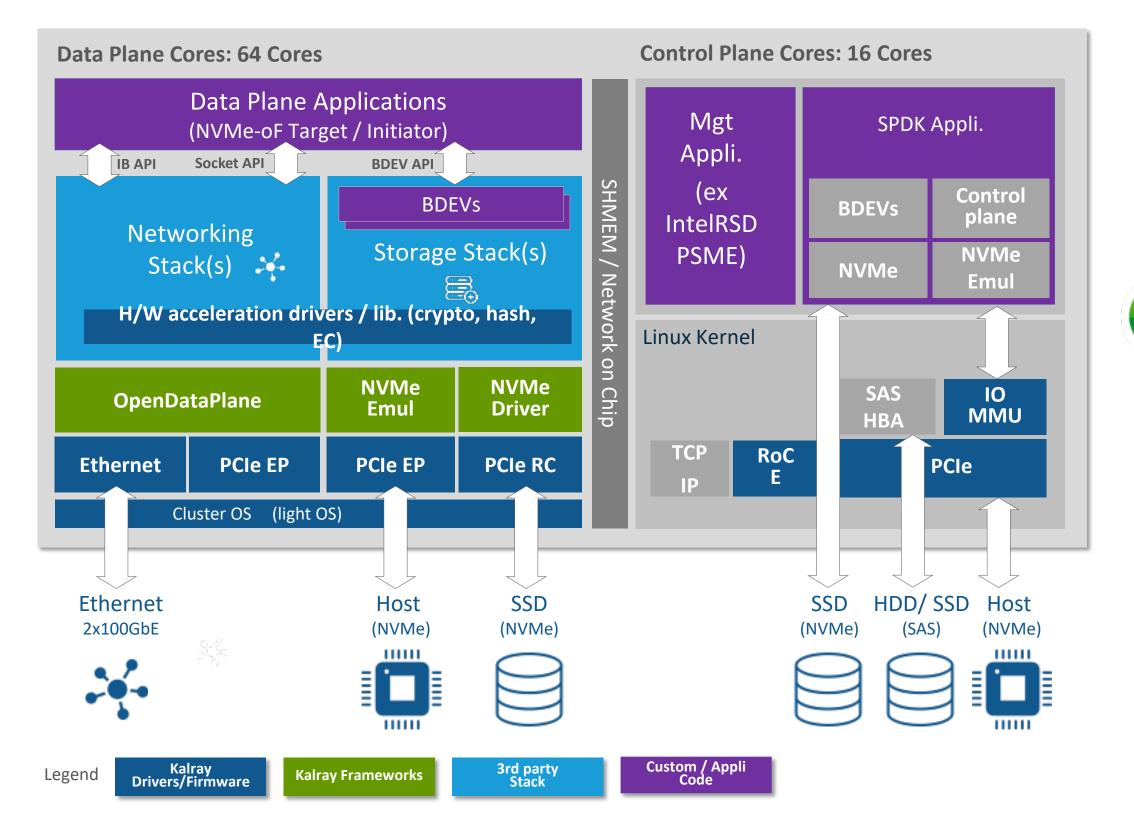
NVMe emulation (up to 256 controllers with SR-IOV)

NVMe I/O queues data access









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A complete & modular software framework

 Based on an optimized SPDK for both data plane
 AND control plane

• Open to partners

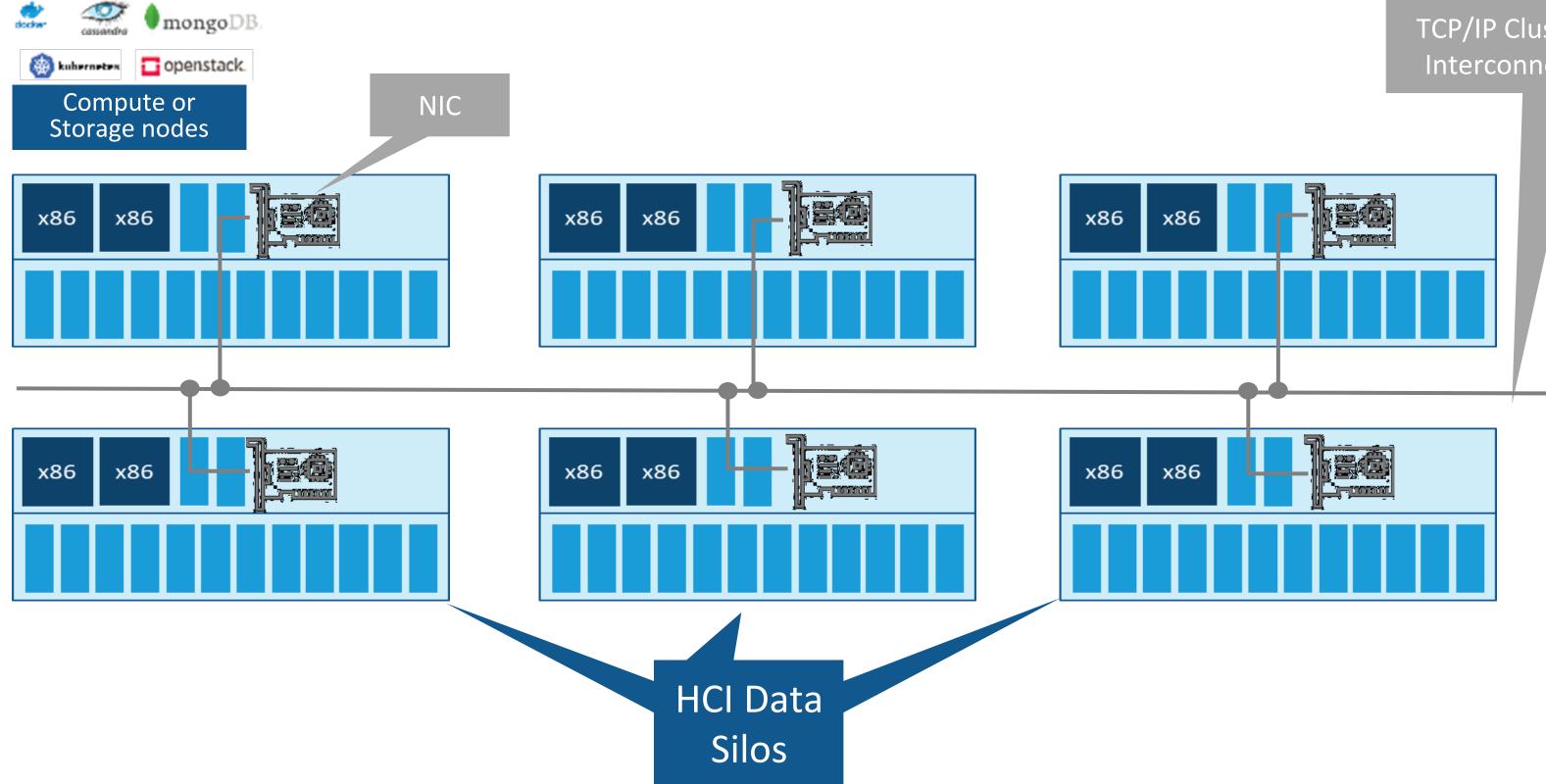
# USE CASE: Future HyperConverged Infrastructure

# $MPPA^{(R)}$

The Processor at the Heart of Intelligent Systems



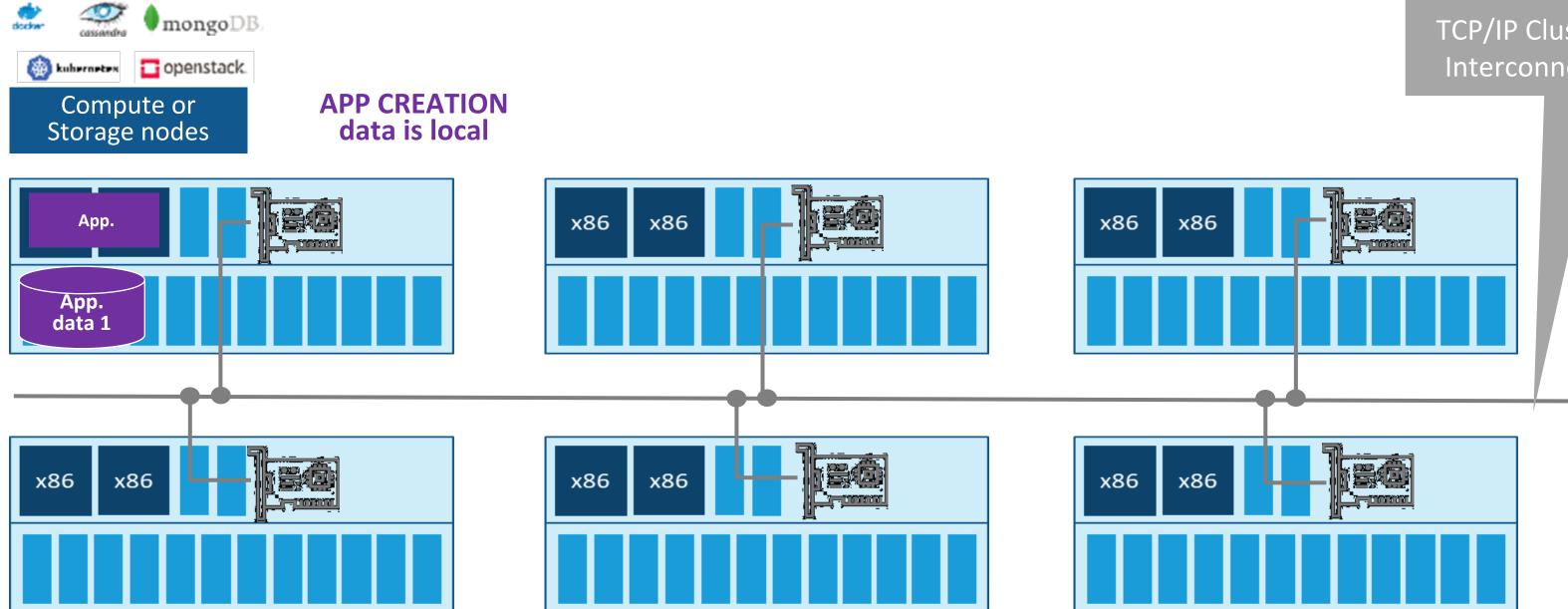
## **CURRENT HCI TOPOLOGY HCI Silos Imposes Disaggregation by Software**



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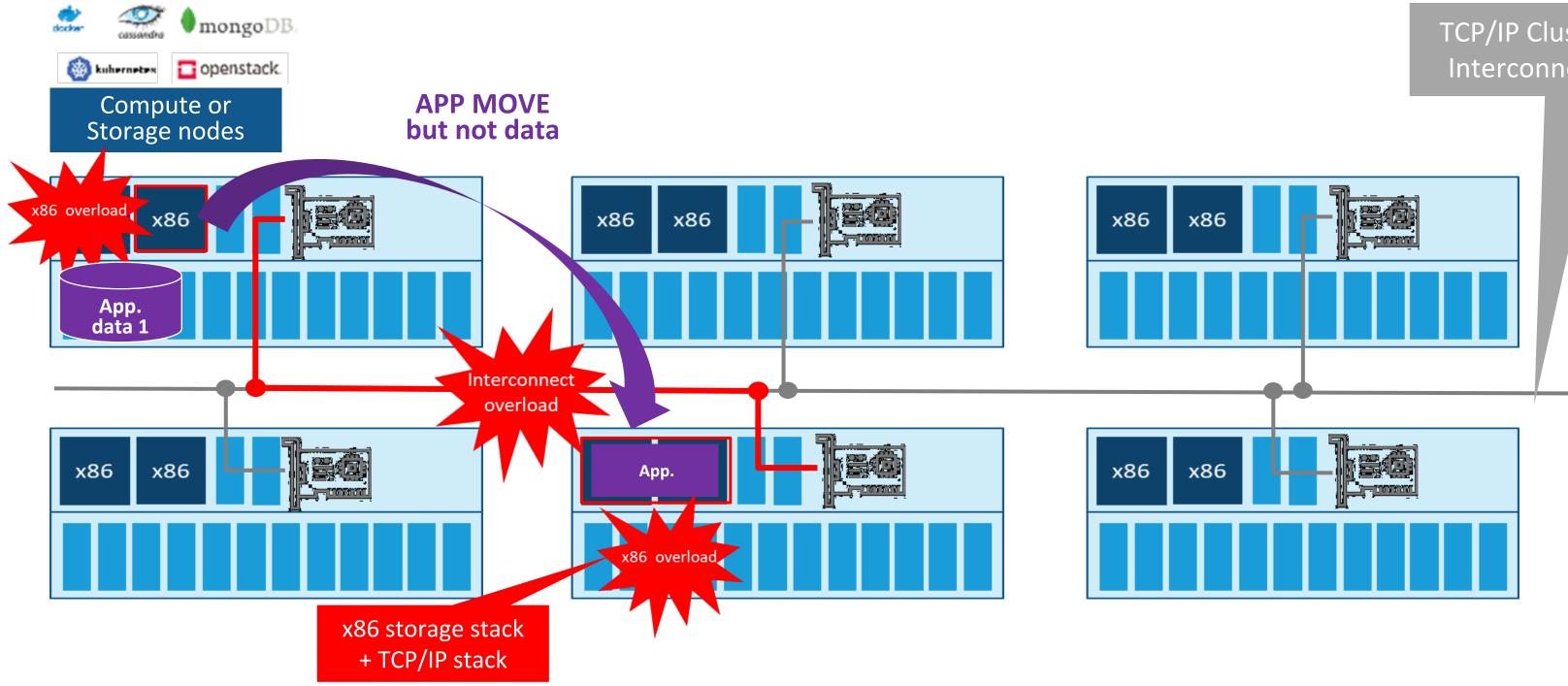
## **CURRENT HCI TOPOLOGY** VMs / Services are Spread across HCI Silos



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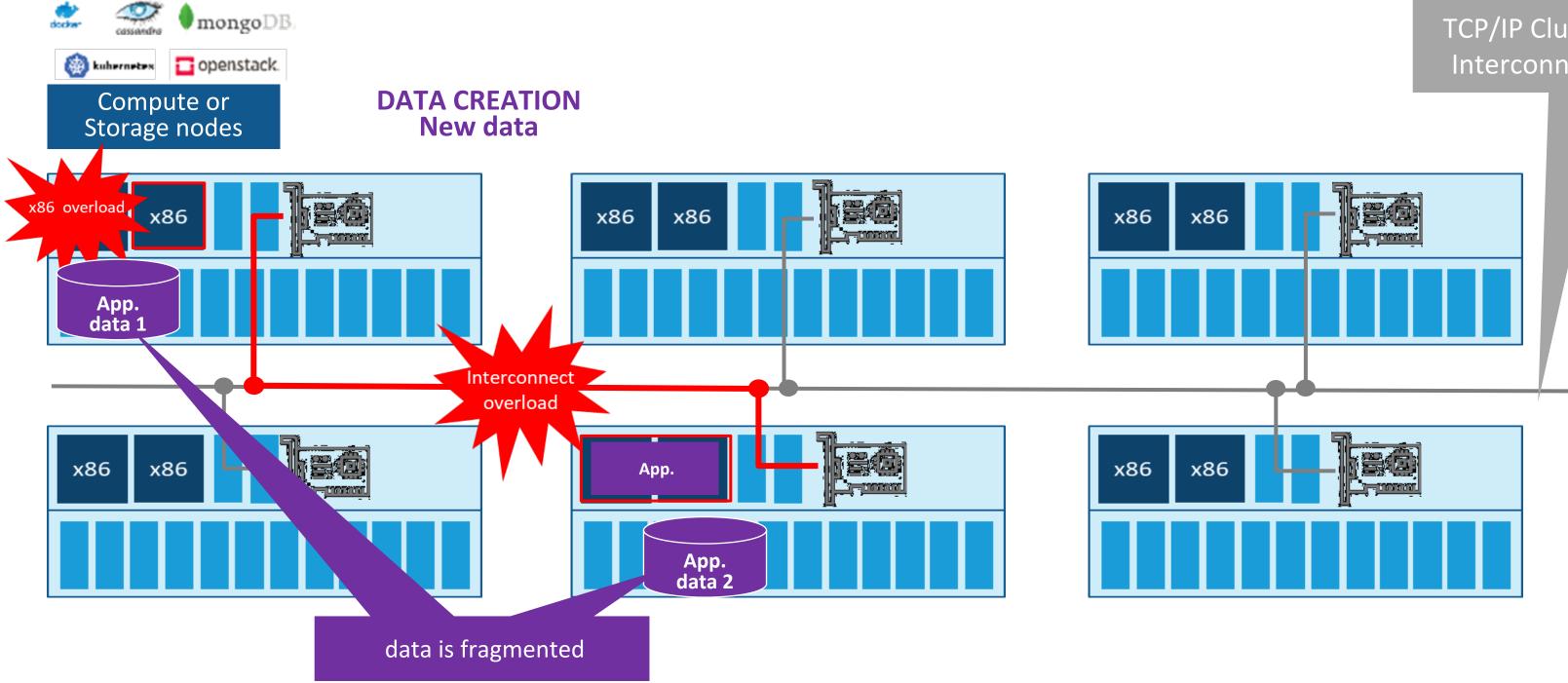
## **CURRENT HCI TOPOLOGY** Impact: Overload of Interconnect and CPUs



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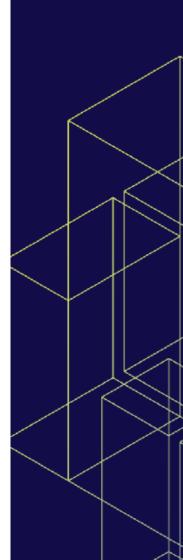


### **CURRENT HCI TOPOLOGY** Fragmented Data Set

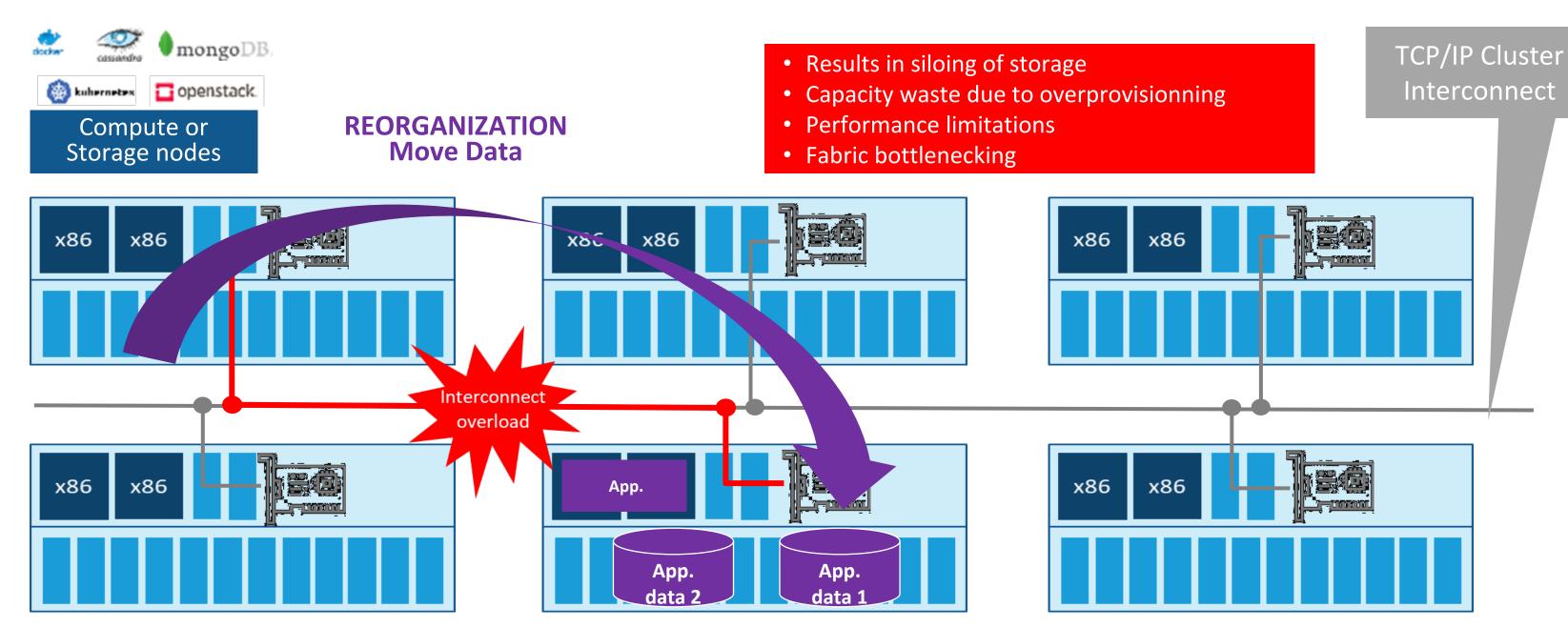


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SD@ 



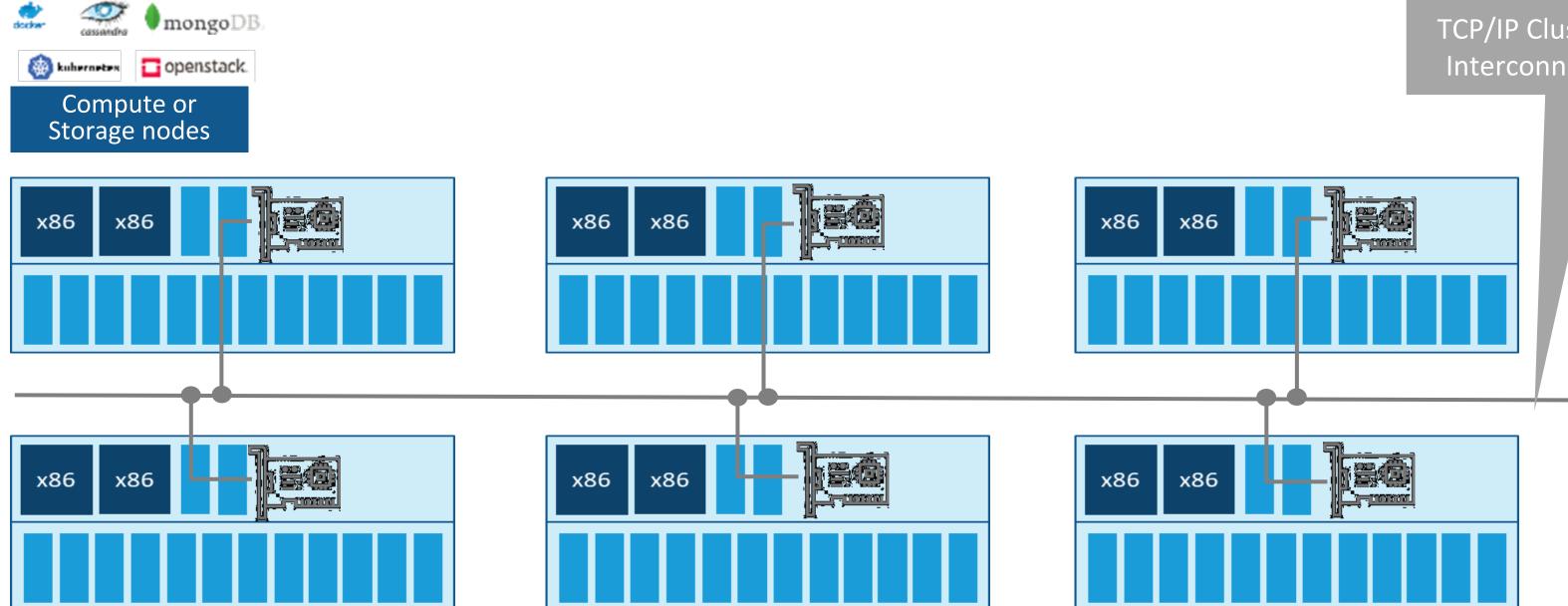
### CURRENT HCI TOPOLOGY Data Relocation is Compulsory



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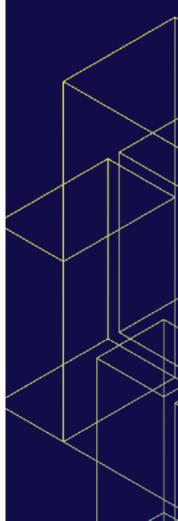


### **HCI WITH NVME-OF NVMe-oF Removes Some Boundaries**

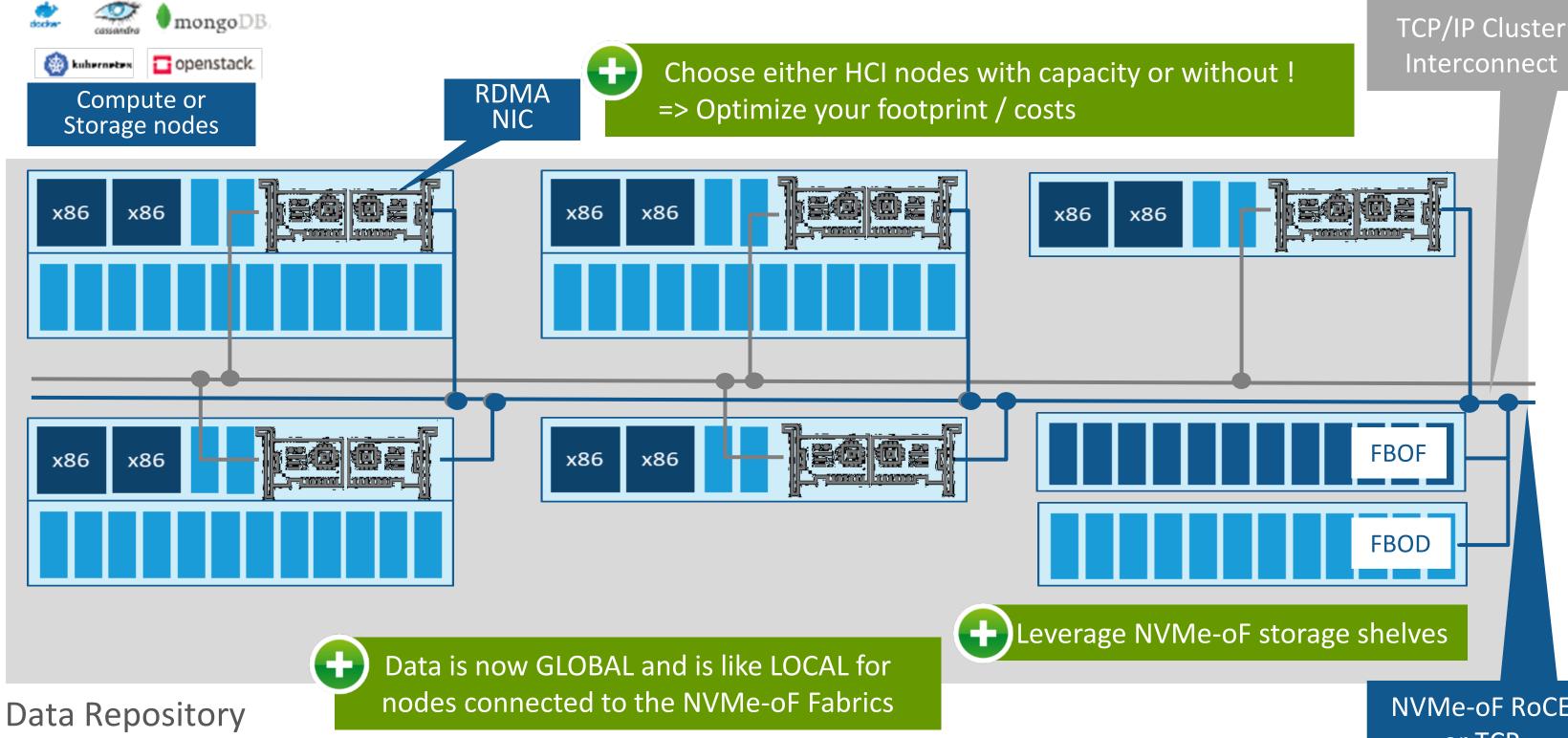


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### HCI WITH NVMe-oF Leveraging NVMe-oF Storage Appliances



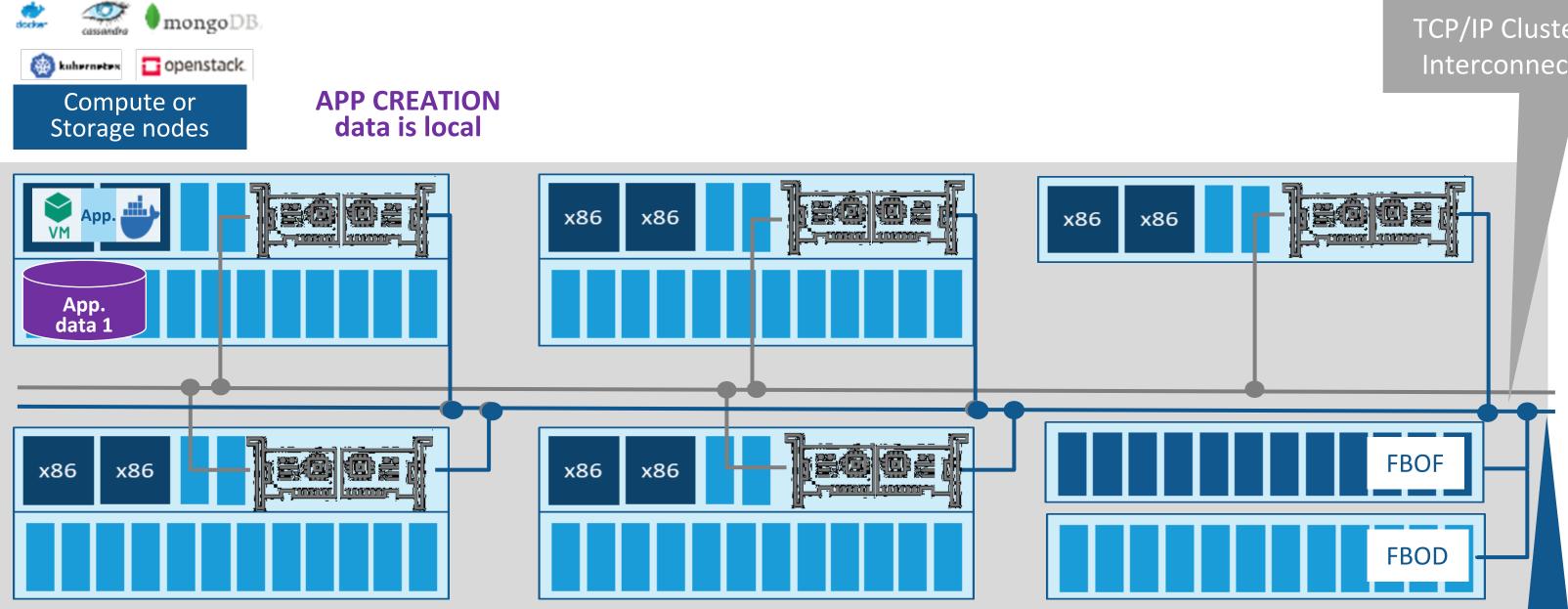
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NVMe-oF RoCE or TCP Interconnect

SD @ 

### HCI WITH NVMe-oF **NVMe-oF Removes Some Boundaries**



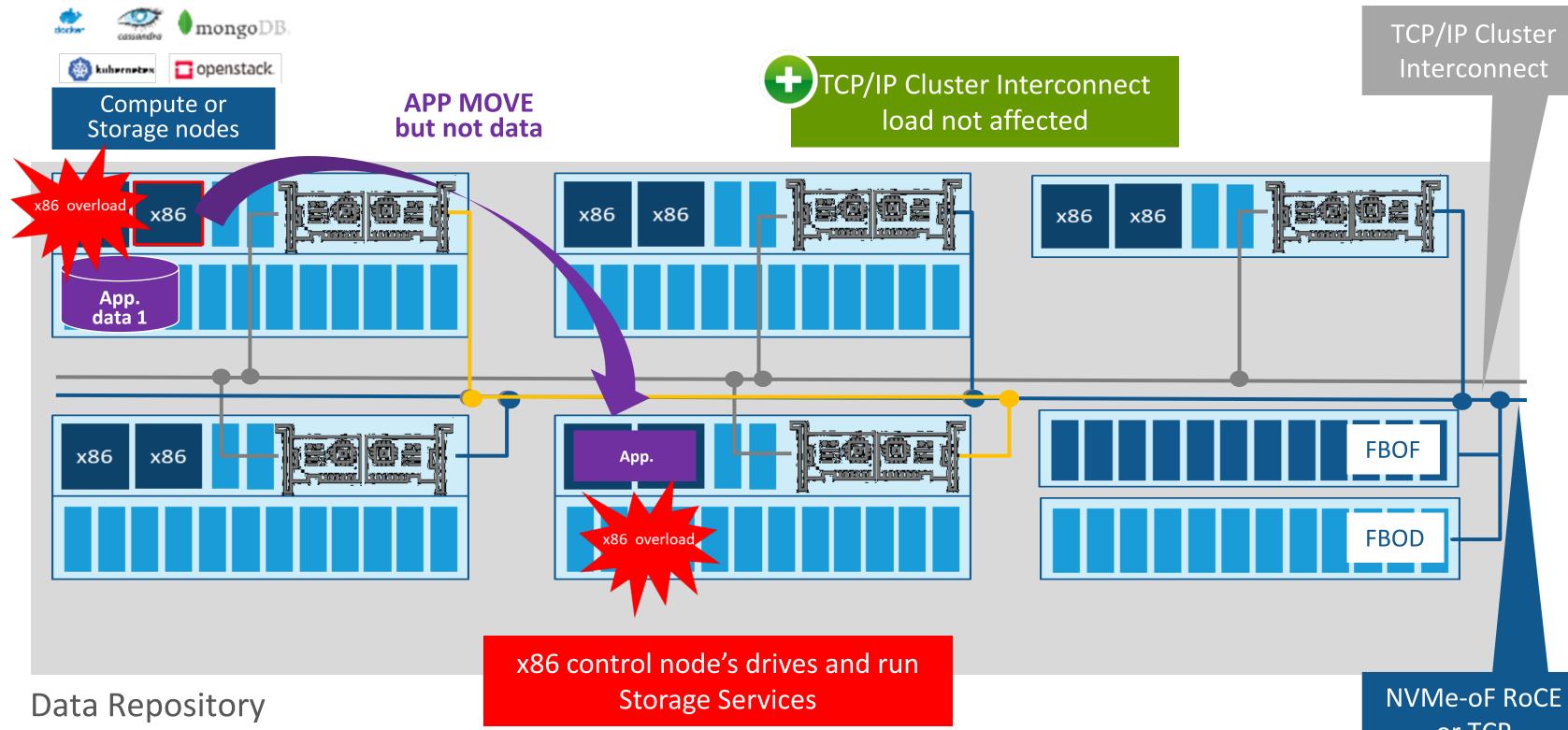
Data Repository

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#### TCP/IP Cluster Interconnect

NVMe-oF RoCE or TCP Interconnect

### HCI WITH NVMe-oF NVMe-oF Removes Interconnect Overload but ...

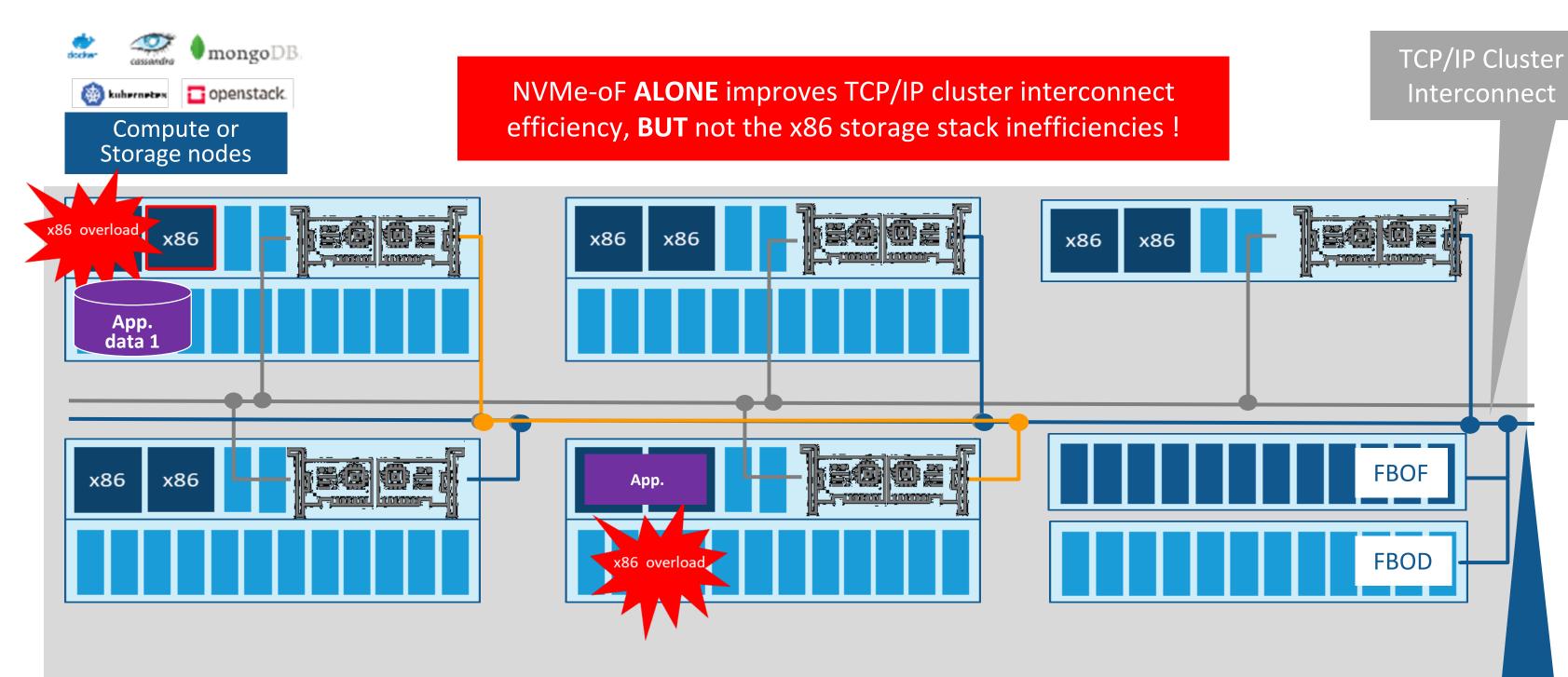


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TCP/IP Cluster Interconnect

or TCP Interconnect

### HCI WITH NVMe-oF **NVMe-oF** Limitations



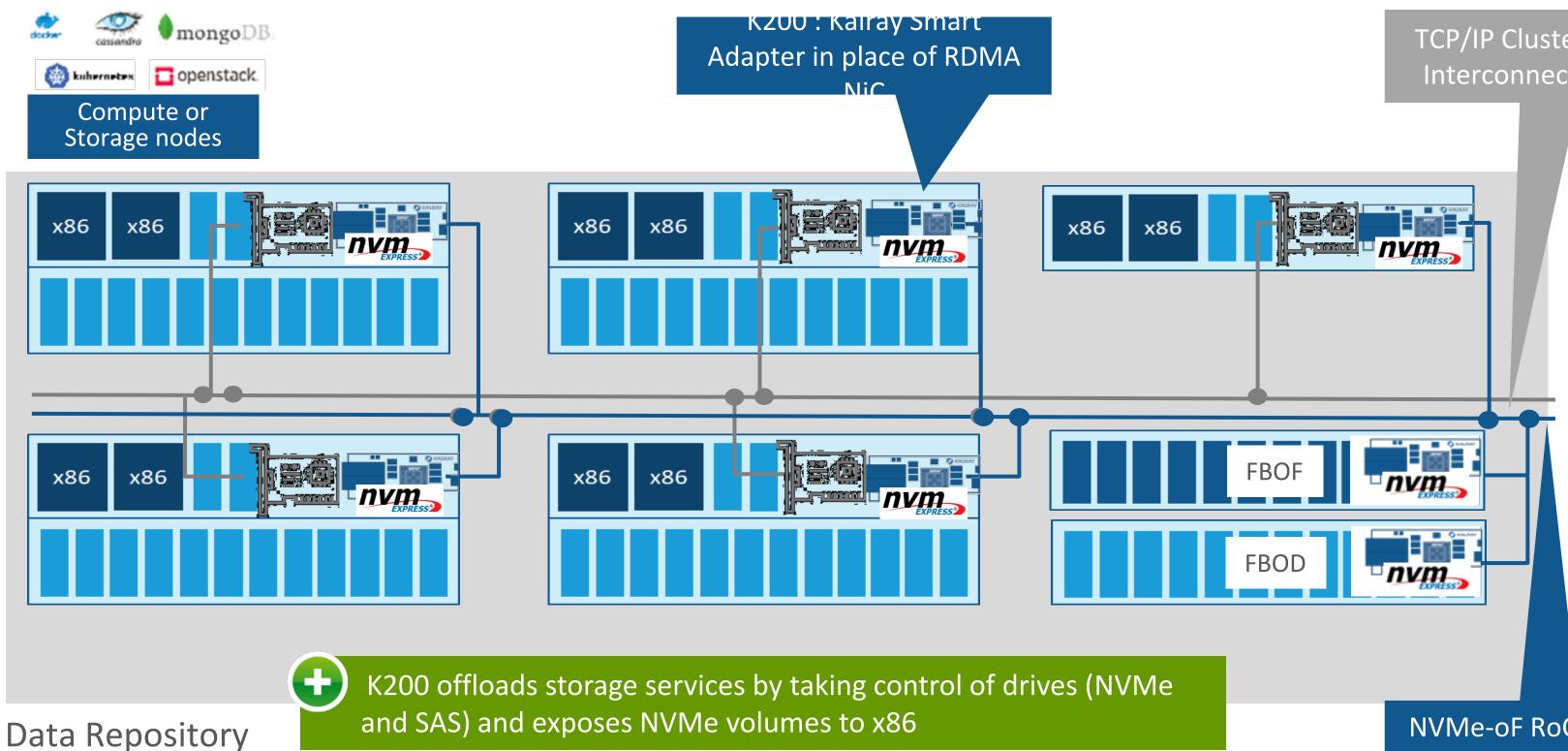
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#### NVMe-oF RoCE or TCP Interconnect

### HCI WITH KALRAY Kalray Smart Adapter Enables New HCI Topology

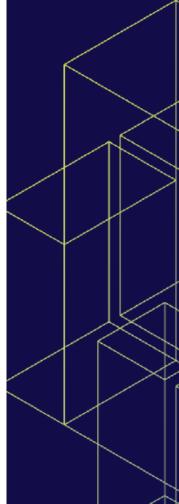


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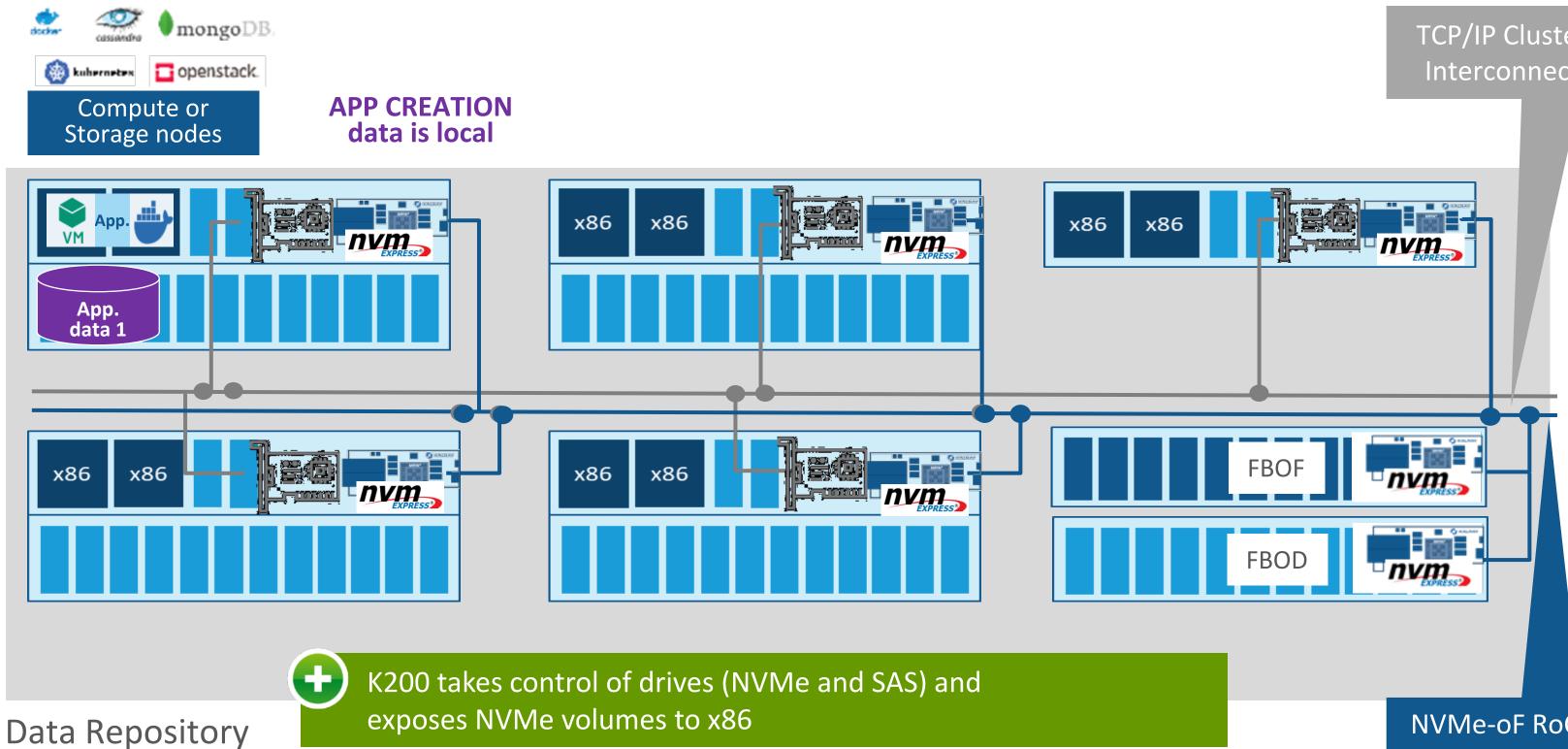
#### **TCP/IP** Cluster Interconnect

NVMe-oF RoCE or TCP Interconnect





### HCI WITH KALRAY **Drives are Under Kalray Storage Adapter Control**



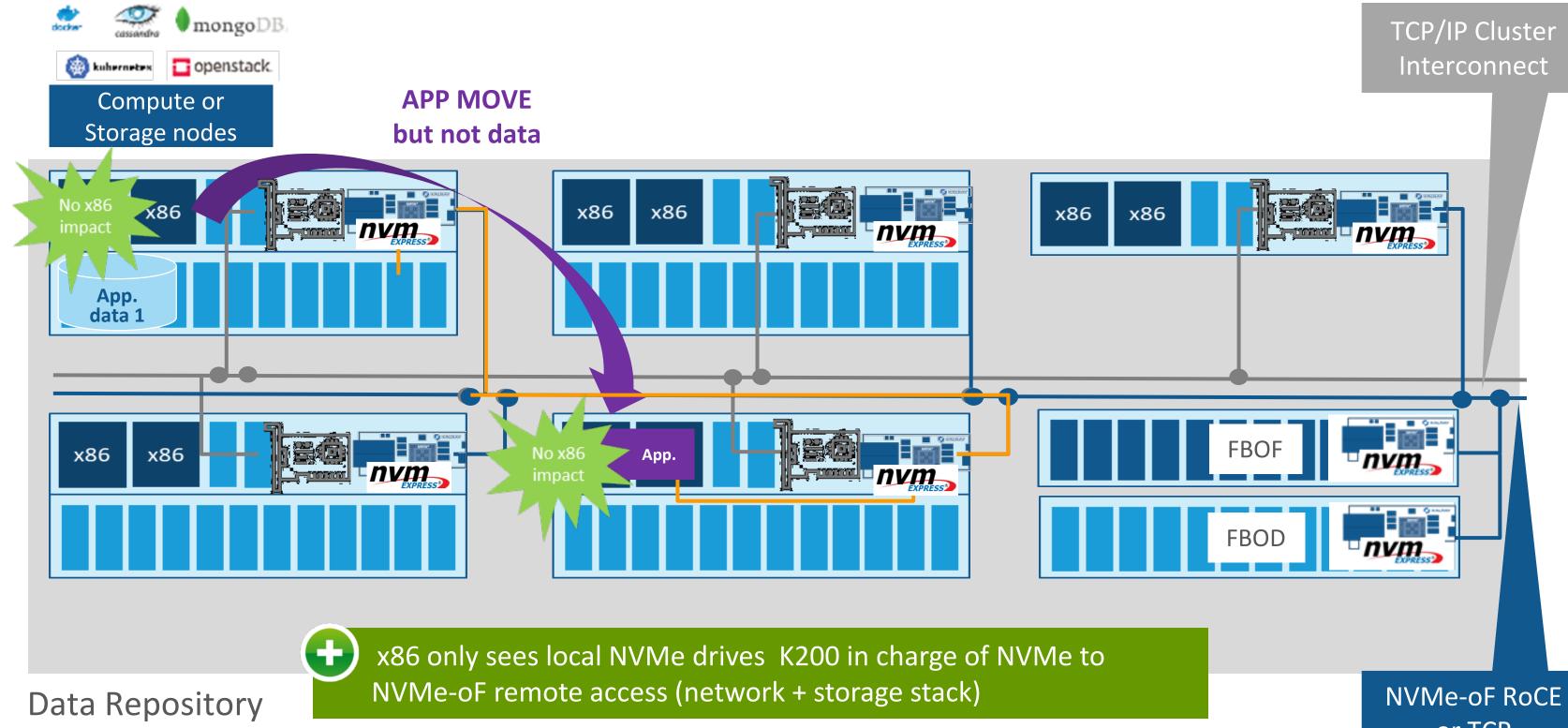
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#### TCP/IP Cluster Interconnect

NVMe-oF RoCE or TCP Interconnect



### **HCI WITH KALRAY** Nodes Only See Local NVMe Drives

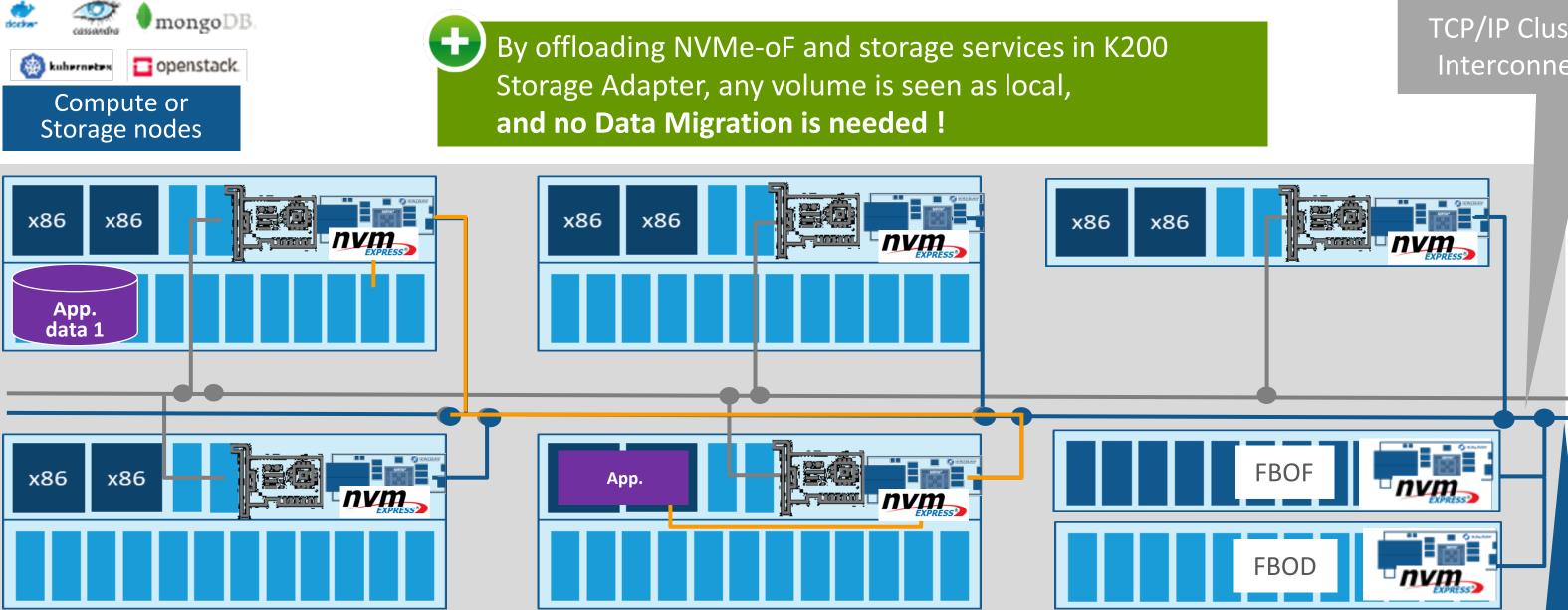


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#### TCP/IP Cluster Interconnect

or TCP Interconnect

### HCI WITH KALRAY **No More Data Migration Required**



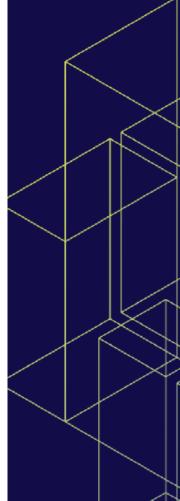
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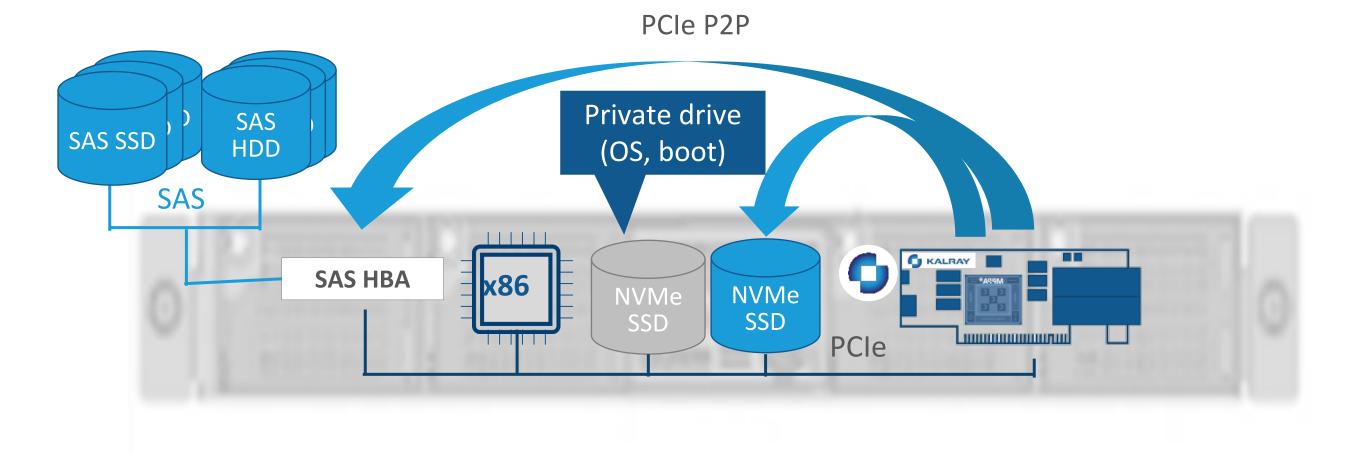
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#### TCP/IP Cluster Interconnect

NVMe-oF RoCE or TCP Interconnect





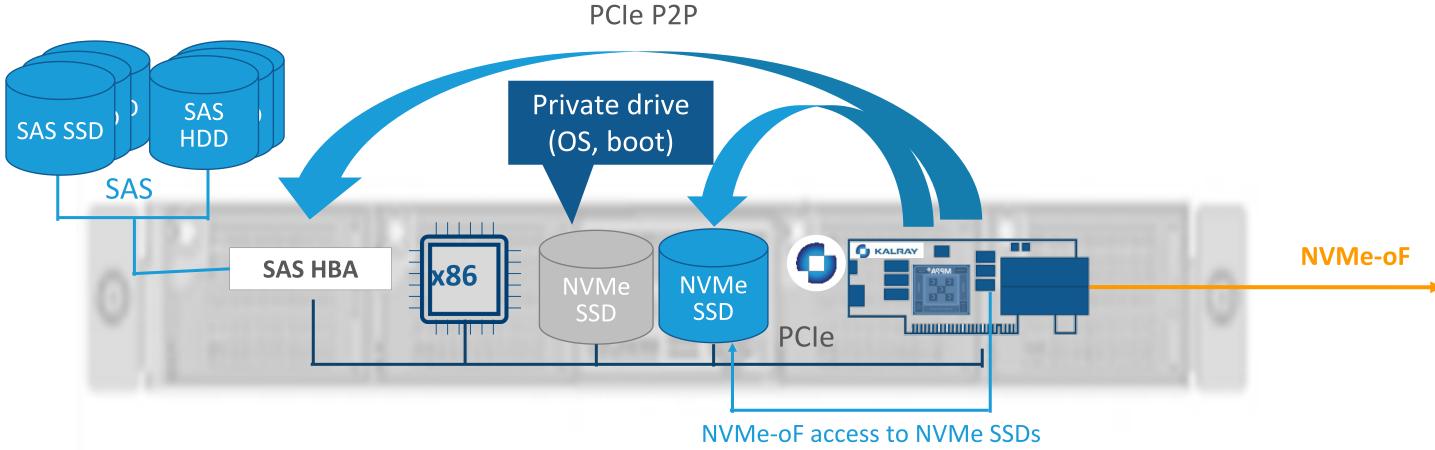


#### K200 Smart Adpater offloads x86 from NVMe-oF & storage services

- NVMe-oF Remote access to node's drives (NVMe / SAS) without x86 involvement
- Local access to node's drive (NVMe / SAS) via storage adapter (NVMe emulation)
- Storage Services added by Kalray Adapter :
  - Caching
  - Distributed Erasure Coding
  - High avalability

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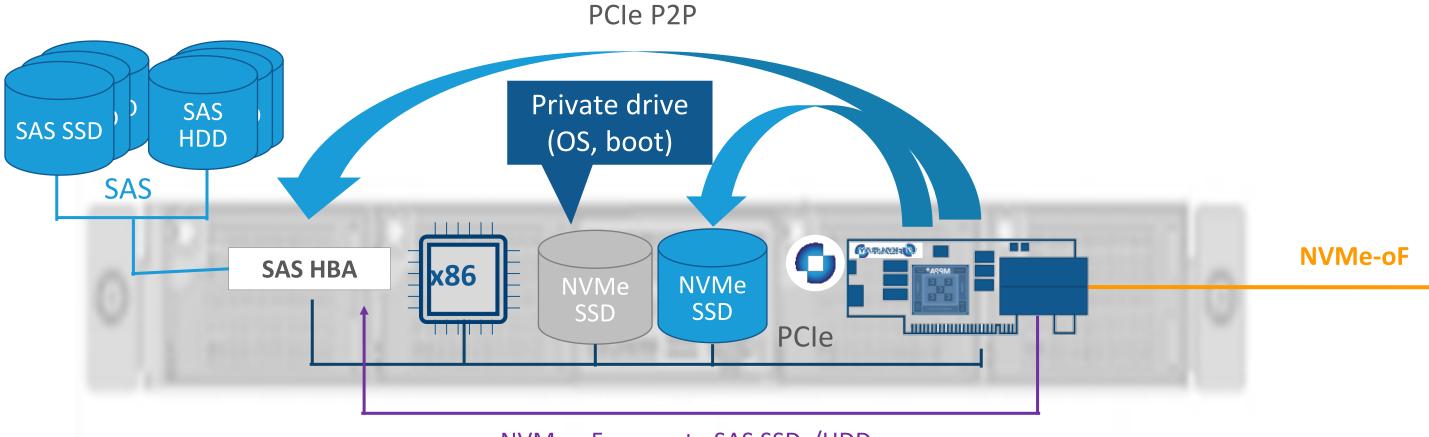


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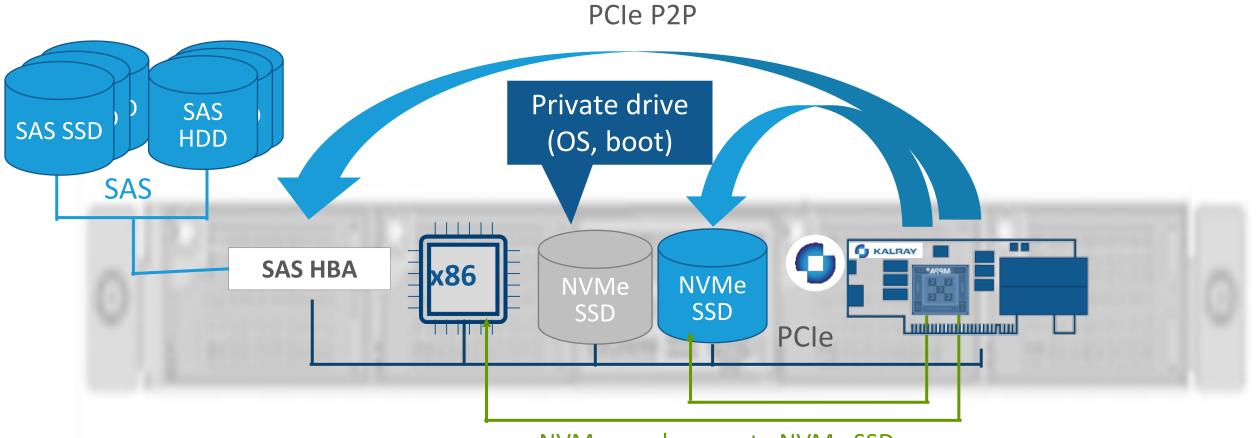
NVMe-oF access to SAS SSDs/HDDs

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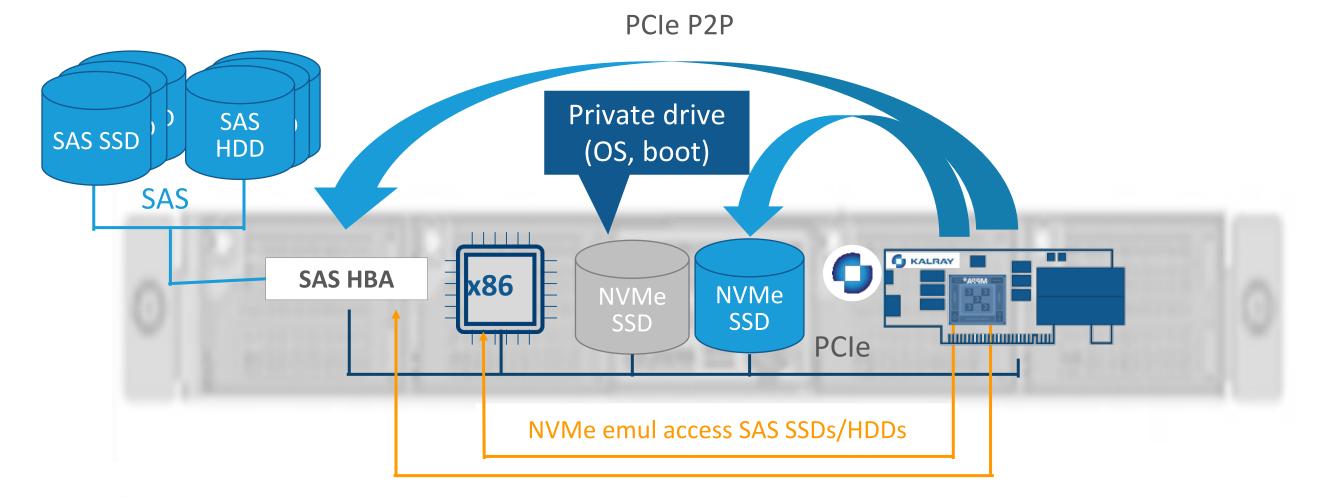
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# Conclusion

### MPPA<sup>®</sup>

The Processor at the Heart

of Intelligent Systems



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## **TOWARD A TRUE & EFFICIENT** COMPOSABLE DISAGGREGATED INFRASTRUCTURE

#### HIGHER PERFORMANCE

- Leverage Kalray cards performance and exploit full NVMe SSD capabilities
- Offload x86 from heavy storage stacks

LOWER COST

- Switch to a true **C**omposable Disaggregated Infrastructure with commodity components
- Optimize HCI nodes efficiency

#### FULLY **FLEXIBLE**

- Fully programmable data plane
- Data Plane additional storage services based on SPDK framework (EC, caching...)

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#### **FUTURE** PROOF

- Leverage standard NVMe-oF protocols
- Compliant with other NVMe-oF appliances
- Ease of in-the-field update



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