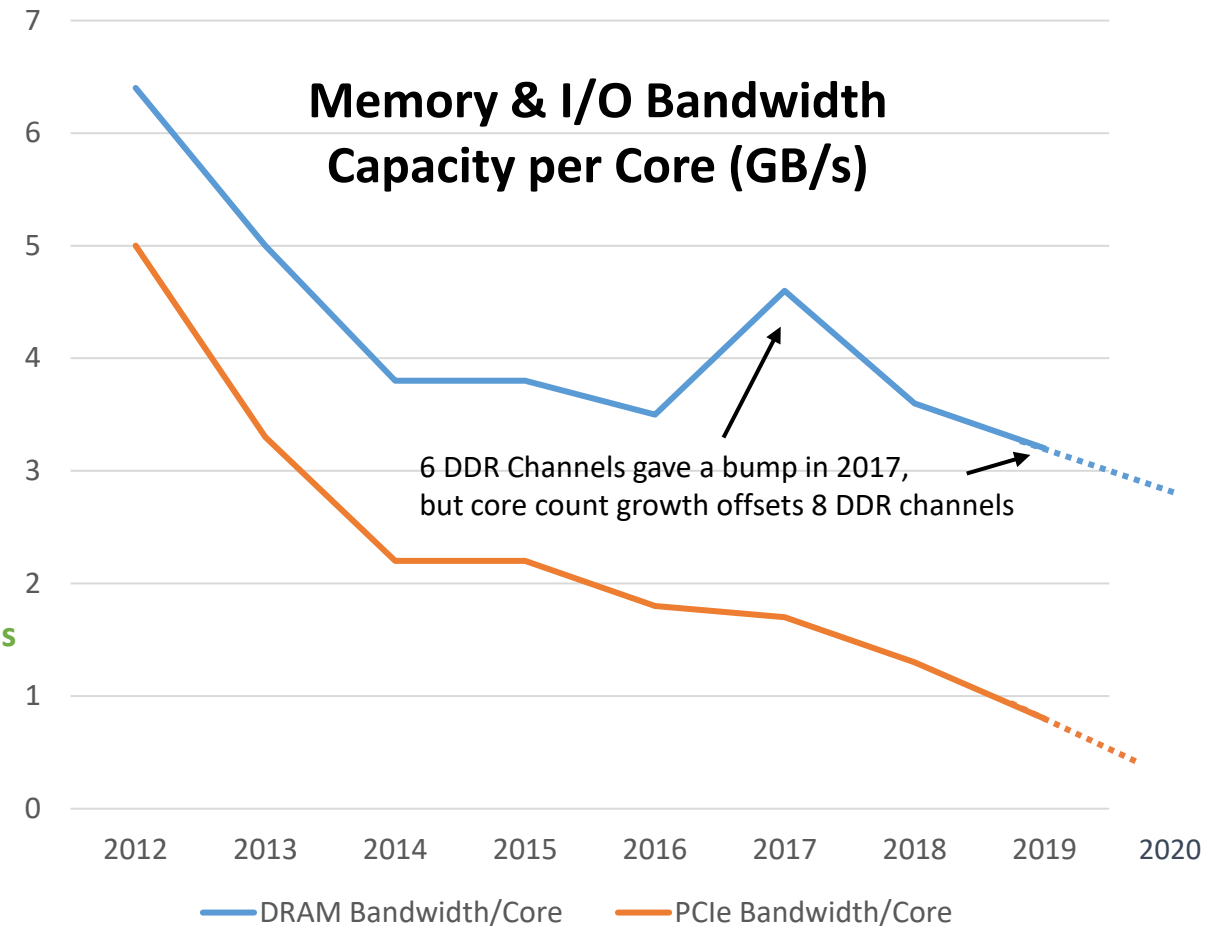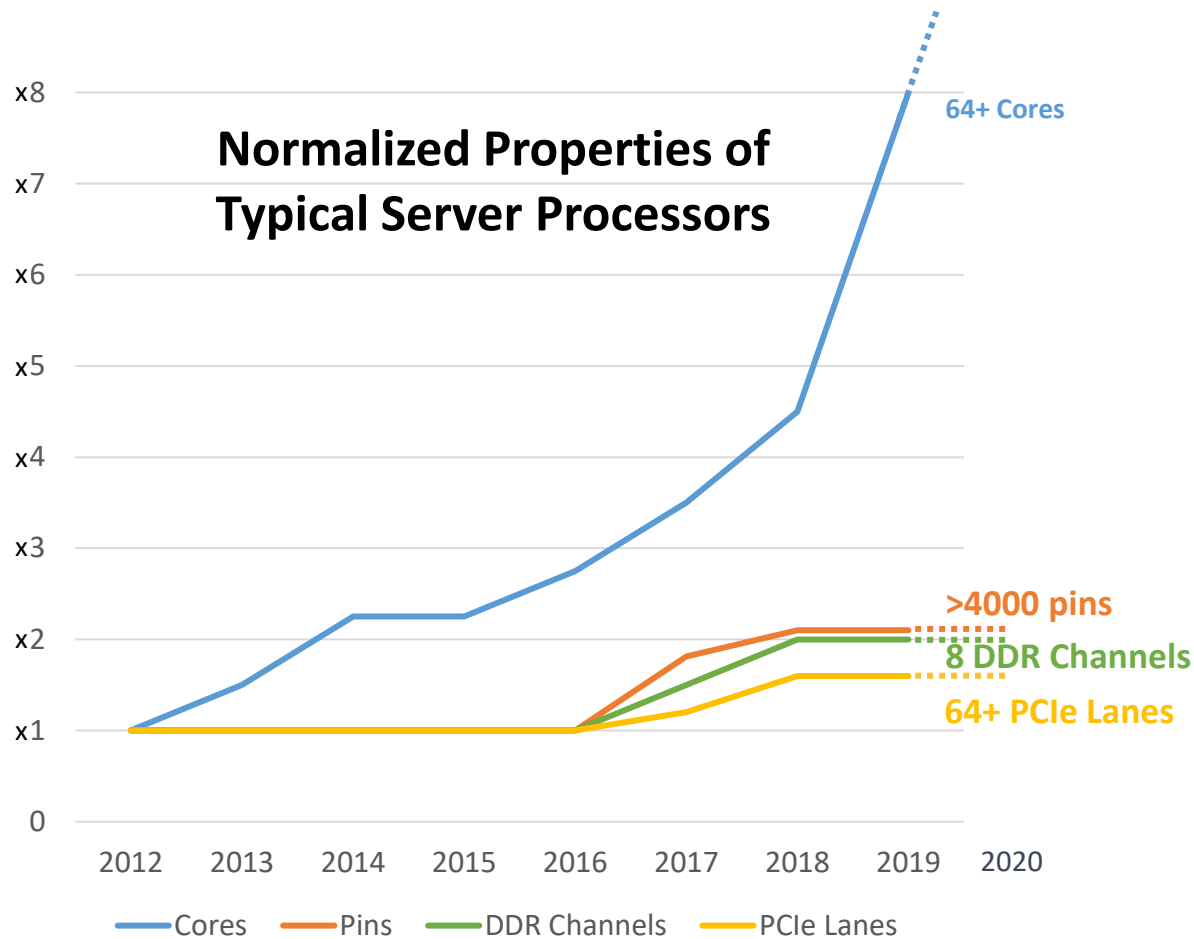# Future of Persistent Memory, DRAM and SSD Form Factors Aligned with New System Architectures

Arthur Sainio

Director, Product Marketing, SMART Modular Technologies
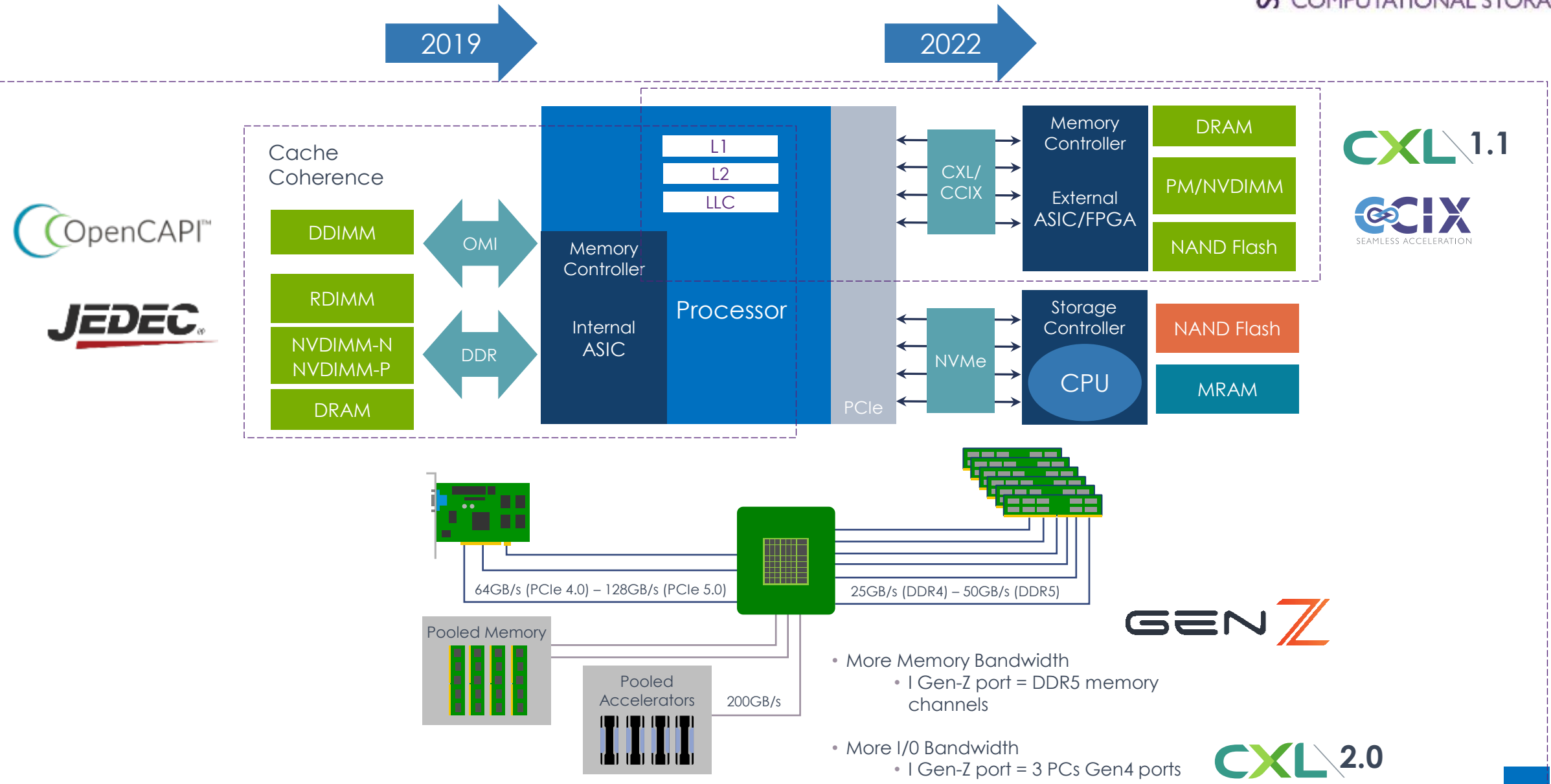
Large Datasets Need Memory that Scales

Normalized Properties of Typical Server Processors

- 64+ Cores
- >4000 pins
- 8 DDR Channels
- 64+ PCIe Lanes

x8, x7, x6, x5, x4, x3, x2, x1, 0

2012 2013 2014 2015 2016 2017 2018 2019 2020

— Cores — Pins — DDR Channels — PCIe Lanes

Memory & I/O Bandwidth Capacity per Core (GB/s)

6 DDR Channels gave a bump in 2017, but core count growth offsets 8 DDR channels

7, 6, 5, 4, 3, 2, 1, 0

2012 2013 2014 2015 2016 2017 2018 2019 2020

— DRAM Bandwidth/Core — PCIe Bandwidth/Core
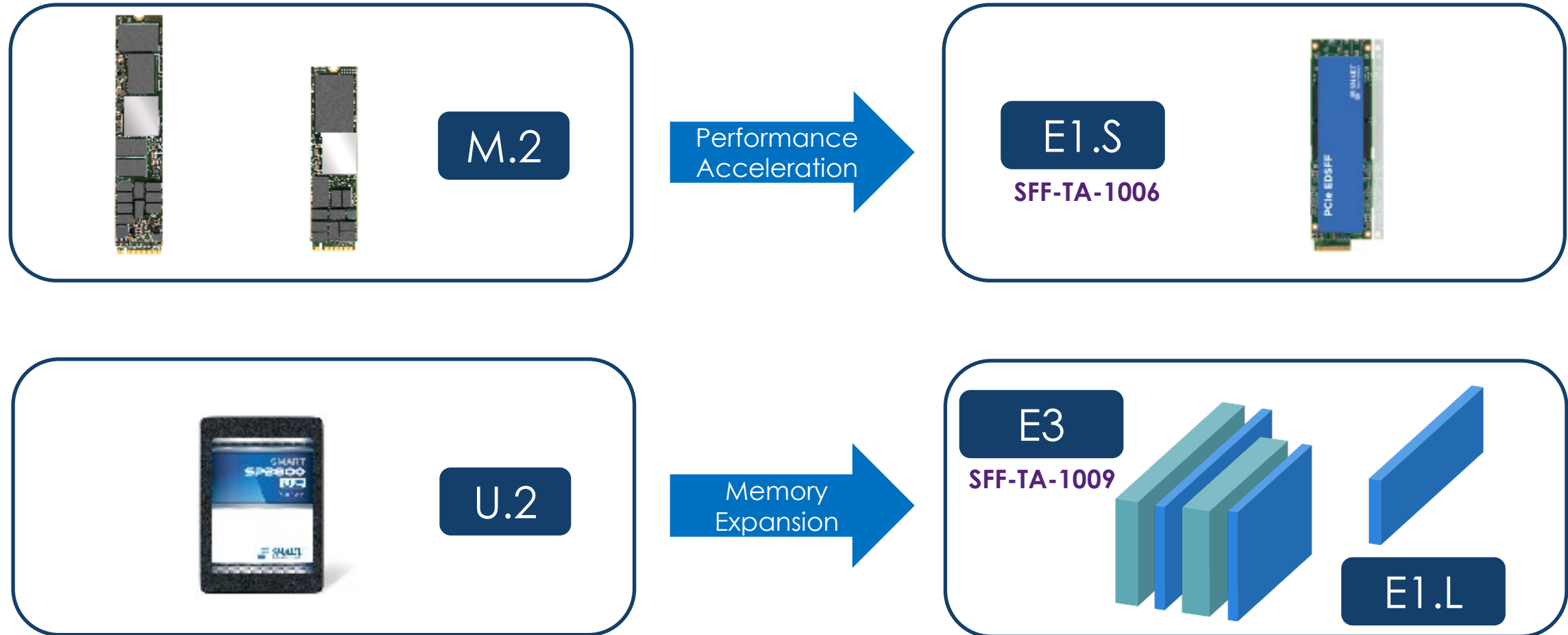
Processor memory and I/O technologies …

… are being stretched to their limits

More than 2X digital data will be created over the next five years compared to the combined amount since the advent of digital storage (Source; IDC, Mar 2020)

Source; Modified from Gen-Z Consortium

Memory and Accelerator Alignment with Fabrics

2019

2022

Cache Coherence

OpenCAPI™

JEDEC®

DDIMM

RDIMM

NVDIMM-N
NVDIMM-P

DRAM

OMI

DDR

Memory Controller

Internal ASIC

Processor

L1

L2

LLC

PCIe

CXL/ CCIX

NVMe

Memory Controller

External ASIC/FPGA

DRAM

PM/NVDIMM

NAND Flash

Storage Controller

CPU

NAND Flash

MRAM

CXL 1.1

CCIX
SEAMLESS ACCELERATION

64GB/s (PCIe 4.0) – 128GB/s (PCIe 5.0)

25GB/s (DDR4) – 50GB/s (DDR5)

Pooled Memory

Pooled Accelerators

200GB/s

GEN Z

- More Memory Bandwidth
  - I Gen-Z port = DDR5 memory channels

- More I/0 Bandwidth
  - I Gen-Z port = 3 PCs Gen4 ports

CXL 2.0

Source; Modified from Intuitive Cognition Consulting

Form Factor Migration

M.2

Performance Acceleration

E1.S
SFF-TA-1006

U.2

Memory Expansion

E3
SFF-TA-1009

E1.L

Performance

Direct attached
(Parallel Bus)
100's of GB
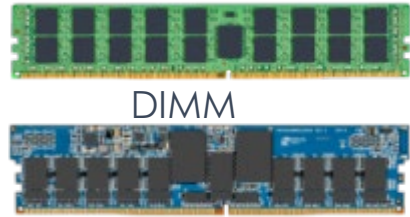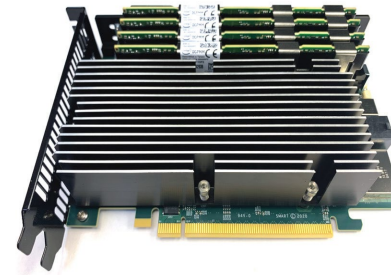
Serial attached
and PCIe attached
100's of GB to TB's

Network Attached
TB's to PB's

DIMM

NVDIMM-N, NVDIMM-P
(Persistent)

E1.S (x4)   E1.S (x8)   E3.S (x16)   PCIe AIC (x16)   OpenCAPI DDIMM

ZMM

	DDR DIMM	E1.S 1C (x4)	E1.S 2C (x8)	E3.S | AIC (x16)	E3 with x8 (2C)	**Across network**
Current Generation *	DDR4@3200 25.6GB/s	PCIe-Gen4-x4 7.8GB/s	PCIe-Gen4-x8 15.7GB/s	PCIe-Gen4-x16 31.5GB/s	OMI 25.6 GB/s 8 lanes	RDMA (Fabric and work load dependent)
Future Generation **	DDR5@4800 63.0GB/s	PCIe-Gen5-x4 15.7GB/s	PCIe-Gen5-x8 31.5GB/s	PCIe-Gen5-x16 63.0GB/s	DDR5 DDIMM (TBD) GB/s	Gen-Z, NVMe-oF (TBD)

* Source(s): https://en.wikipedia.org/wiki/PCI_Express#History_and_revisions
https://en.wikipedia.org/wiki/DDR4_SDRAM#JEDEC_standard_DDR4_module
https://www.smartm.com/media/press-releases/smart-modular-to-showcase-its-ddr4-differential-dimm-at-the-flash-memory-summit
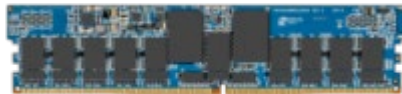
** Source(s): https://www.tomshardware.com/news/ddr5-6400-ram-benchmarks-major-performance-gains-ddr4
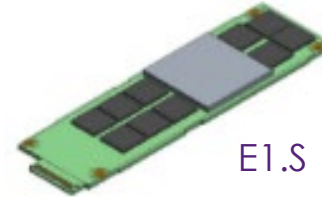
Latency

Direct attached (Parallel Bus) 100's of GB

Serial attached and PCIe attached 100's of GB to TB's

Network Attached TB's to PB's
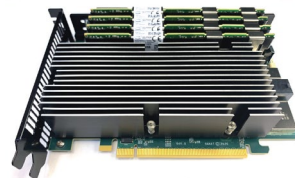
DIMM

NVDIMM-N, NVDIMM-P

JEDEC

DDIMM (40ns latency)

OpenCAPI

Cache Coherent AIC

E1.S

CCIX SEAMLESS ACCELERATION

XMM, NV-XMM

CXL Compute Express Link

GEN Z

ZMM

GEN Z

<100ns   <350ns   <800ns
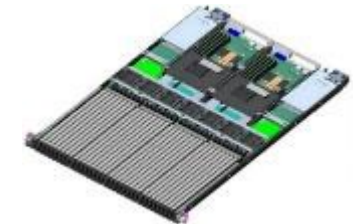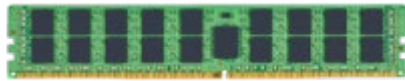
Form Factors

Direct attached
(Parallel Bus)
100's of GB

Serial attached
and PCIe attached
100's of GB to TB's

Network Attached
TB's to PB's

DIMM

NVDIMM-N, NVDIMM-P

E1.S (x4)

E1.S (x8)

E3.S (x16)

E3.S (x8)

|	DDR4 DIMM	E1.S with x4 (1C)	E1.S with x8 (2C)	E3.S with x16 (4C)	E3 with x8 (2C)	Network Card
Pins	288 pins (64 data, 87 sideband, rest power)	56 pins (16 diff-data, 16 sideband, 24 power)	84 pins (32 diff-data, 18 sideband, 34 power)	140 pins (64 diff-data, 24 sideband, 52 power)	84 pins (32 diff-data, 18 sideband, 34 power)	Media and protocol specific
Connect or (LxW)	142.0mm x 6.5mm	23.8mm x 6.0mm	35.6mm x 6.0mm	57.0mm x 6.0mm	35.6mm x 6.0mm	SFP/QSFP/…
Power	Input voltage=1.2V VPP 2.5	Input voltage 12V Vaux 3.3 (optional)	Input voltage 12V Vaux 3.3 (optional)	Input voltage 12V Vaux=3.3 (optional)	Input voltage 12V	Vendor specific

Bandwidth

Current Generation configuration
Dual socket server with **64 core CPU** and
12 x **DDR4** channels populated with 128GB DDR4
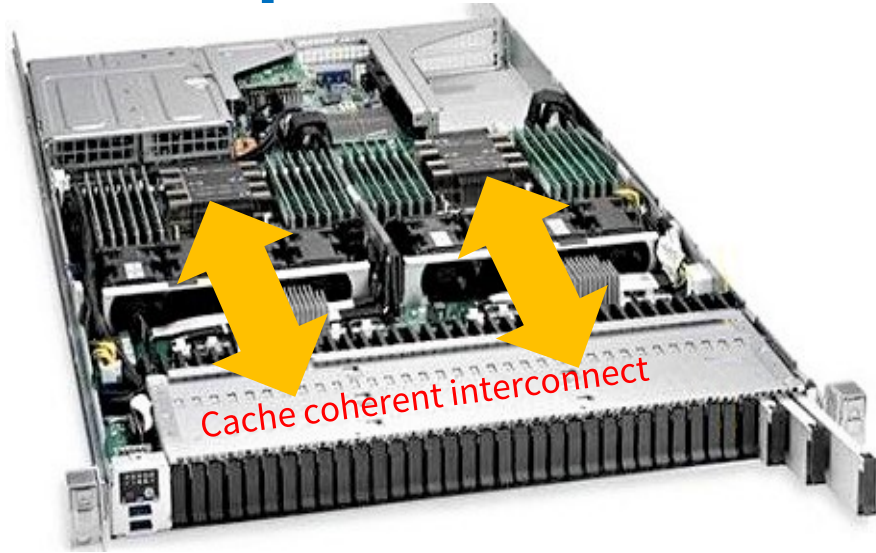DIMMs in 2 DIMMs/Channel

Future Generation configuration – 2022
Dual socket server with **96 core CPU** and
12 x **DDR5** channels populated with
128GB DDR5 DIMMs in 2 DIMMs/Channel

8 x 256GB CXL
memory modules
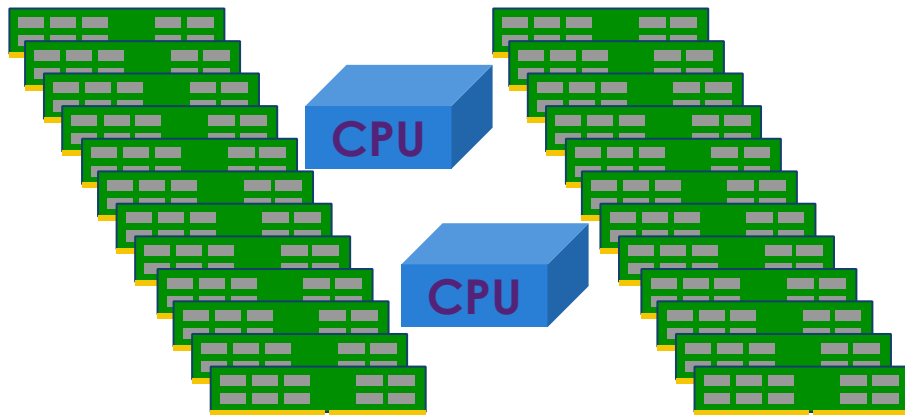
- Total Memory = 3TB per server
- Theoretical maximum bandwidth of 614GB/s
- Bandwidth per core = 4.79GB/s
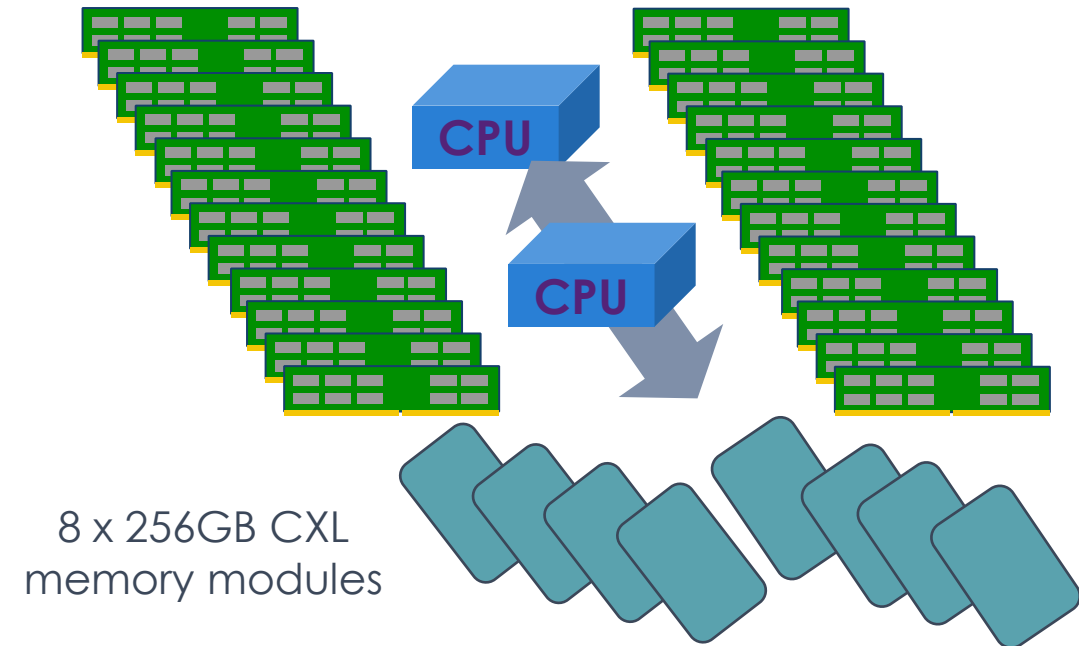
- Total Memory = 3TB (DDR5) **+ 2TB (CXL)** per server
- Theoretical maximum bandwidth of 768GB/s (DDR5)+ 252GB/s (CXL)
- Bandwidth per core = 5.3GB/s **(higher even with more CPU cores)**

Source: https://www.tomshardware.com/news/what-we-know-ddr5-ram,39079.html

E1.S and E1.L for Memory Acceleration and Expansion

Cache coherent interconnect

PCIe EDSFF

SMART

KIOXIA Data Center XD6 NVMe SSD

KIOXIA Data Center XD6 NVMe SSD
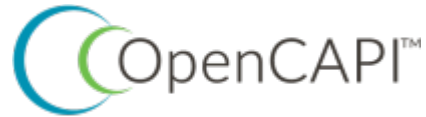
SMART

Feature	Description
Host Interface	• Data: PCIe x4,x8 • Sideband: SMBus (I2C) • Wake-up, Low-power (PWRDIS), ...
Memory	64-128GB with DDR4 or DDR5
Protocols	NVMe, CXL, CCIX, Gen-Z
Power	• Multiple profiles from 12,16, 20, 25W • Completely bus powered: 12V (main), 3.3V Aux • Supports low power modes (CLKREQ#, PWRDIS signaling)
Targeted Use Cases Memory Acceleration and Expansion	Targeted for 1U Servers • 16 – 32 Slots per 1U Server • Improves performance by offloading fixed functions like encryption, compression or Key-Value semantics to Memory modules.

Source: https://www.anandtech.com/show/16248/edsff-form-factor-updates

E3.S and E3.L for Memory Expansion
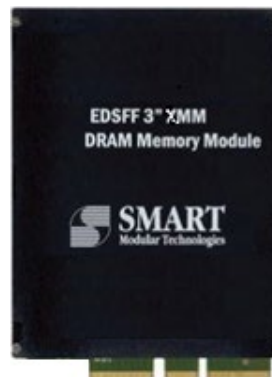
Feature	Description
Host Interface	• Data: PCIe x16 • Sideband: SMBus (I2C) • Wake-up, Low-power (PWRDIS), ...
Memory	Up to 256GB with DDR4 or DDR5 * Non-volatile persistent memory feature could be support on this form-factor using back-up and restore functionality like in NVDIMM-N.
Protocols	NVMe, CXL, CCIX, Gen-Z
Power	• 2 profiles 25W (thin) and 40W (thick) • Bus powered: 12V (main), 3.3V Aux • Supports low power modes (CLKREQ#, PWRDIS signaling)
Targeted Use Cases Memory Expansion	Targeted for 2U Server Enables 4TB – 8 TB of Memory expansion with 16 E3.S modules in single 2U server, achieving better throughput than direct attached DDR4 DIMM.

OpenCAPI High Bandwidth Memory - DDIMM

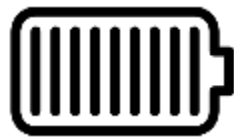| Feature	Description
Host Interface	• OpenCAPI
Memory	• Up to 256GB
Protocols	• OMI – Open Memory Interface • The memory bus is defined with one read port and one write port per channel, each having eight unidirectional differential lanes
Performance	• DDR4-3200 • Latency 40ns • Data throughput rate of 25.6GB/s with 8 lanes • The DDIMM/OMI approach delivers up to 4TB of memory on a server at about 320GB/second or 512GB at up to 650GB/s sustained rates.
Targeted Use Cases	• Targeted for servers • High bandwidth, low latency serial connection for memory, accelerators, network, storage, and other devices like ASICs

NVDIMM for Persistent Memory

Key Features of DDR4 and DDR5 NVDIMM-N

- Operation like DRAM
- Fast recovery from system power loss
- Software overhead can be eliminated

+

Backup Power

Feature	Description
Host Interface	• DDR
Memory	• DDR4 16GB, 32GB • DDR5 32GB, 64GB
Protocol	• JEDEC Compliant DDR4 / DDR5
Features	• Throughput of 25.6GB/s (DDR4) • Latency ~20ns • AES 256 bit Encryption
Targeted Use Cases	• All Flash Arrays, Storage Servers, HPC, AI Training Servers • Needed for very low latency tiering, caching, write buffering, metadata storage, checkpointing • Needed for AI/ML algorithm processing

CXL-based NVDIMM (NV-XMM)

DRAM
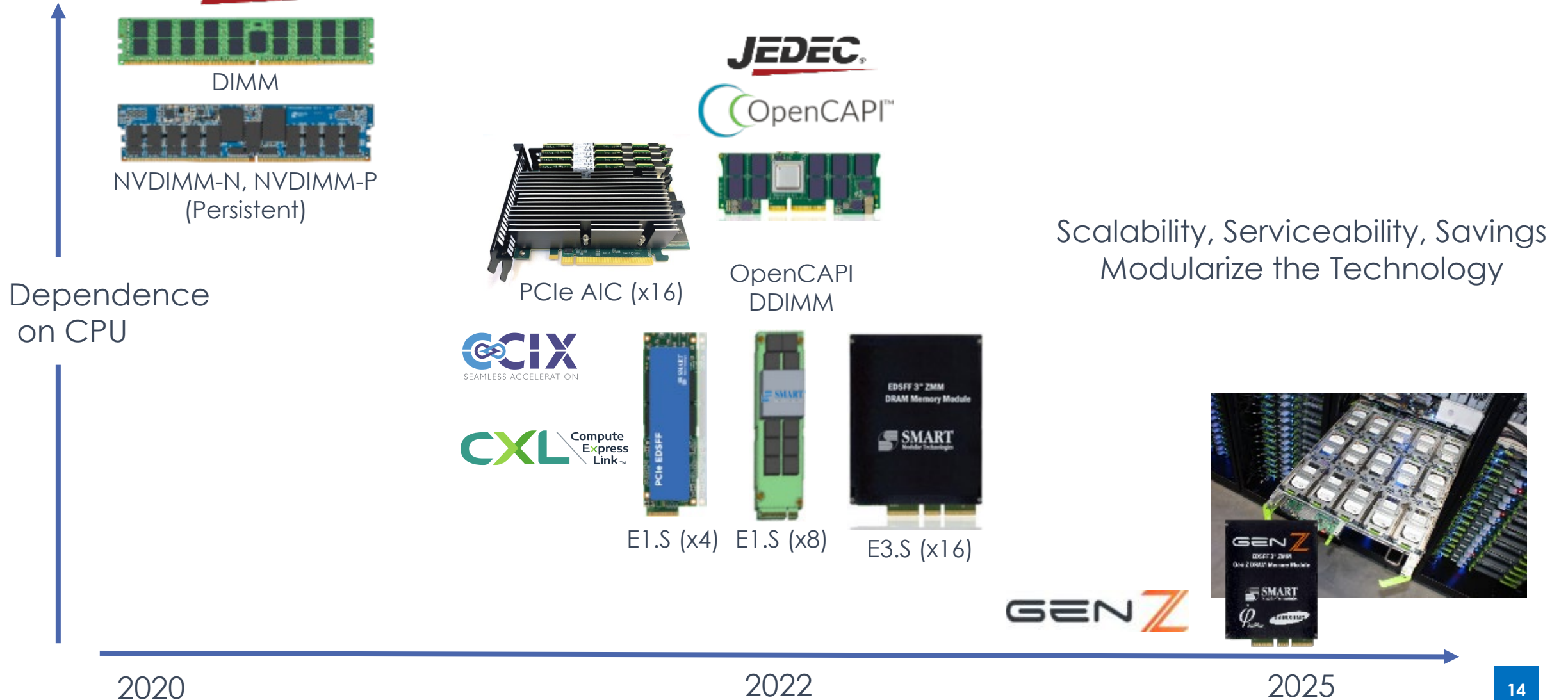
DRAM

CPU

CXL Compute Express Link ™

NVM

NVM

NVM
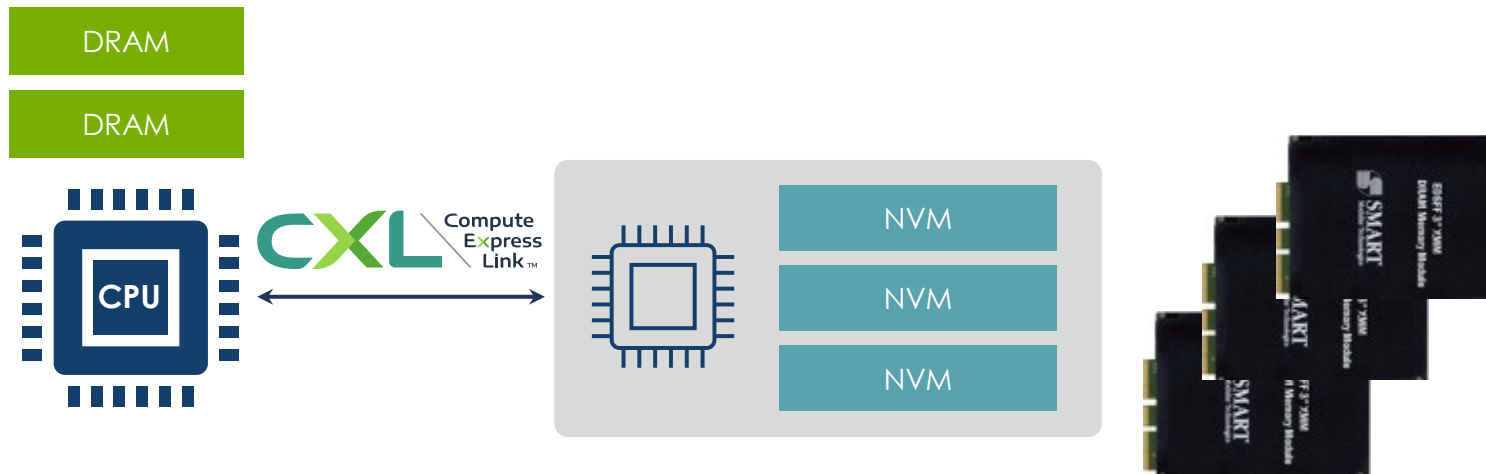
High-speed DRAM with built-in back-up power to back-up data to on-module Flash during power loss.

Source: Modified from PIRL 2019, "Accelerate Everything", Stephen Bates, Eideticom

Source: PIRL 2019, "Accelerate Everything", Stephen Bates, Eideticom

Conclusions

Future of Persistent Memory, DRAM and SSD Form Factors

JEDEC

DIMM

NVDIMM-N, NVDIMM-P
(Persistent)

JEDEC

OpenCAPI™

PCIe AIC (x16)

OpenCAPI
DDIMM

Scalability, Serviceability, Savings
Modularize the Technology

Dependence
on CPU

CCIX
SEAMLESS ACCELERATION

CXL Compute Express Link ™

PCIe EDSFF

SMART

EDSFF 3" ZMM
DRAM Memory Module

SMART
Modular Technologies

E1.S (x4)   E1.S (x8)

E3.S (x16)

GEN Z

2020

2022

2025

Thank you

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