STORAGE DEVELOPER CONFERENCE
SDC 21
BY Developers FOR Developers
Virtual Conference
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A SNIA Event

SmartNICs

The Architecture Battle Between Von Neumann and Programmable Logic

Scott Schweitzer

Agenda

- Sources
- Architecture
- Players
- Market
- Software Today, Hardware Tomorrow
- Additional Important Issues

Speaker Photo Will Be Placed Here

Source for Some Perspectives:

Panel: Von Neumann vs. Programmable Logic SmartNICs: Which is the Dead End?

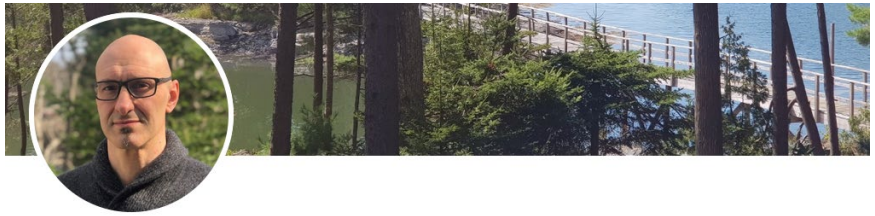
HOT INTERCONNECTS

Speaker Photo Will Be Placed Here

Von Neumann

Cary Ussery · 2nd
Bringing Technology to Life
Pleasanton, California, United States · Contact info

Marvell Semiconductor
Bard College



Mario Baldi · 1st
Distinguished Technologist at Pensando Systems
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Pensando Systems
Politecnico di Torii

Michael Kagan · 1st
CTO at NVIDIA
Haifa, Israel · Contact info

NVIDIA
Technion - Israel Institute of Technology

Programmable Logic

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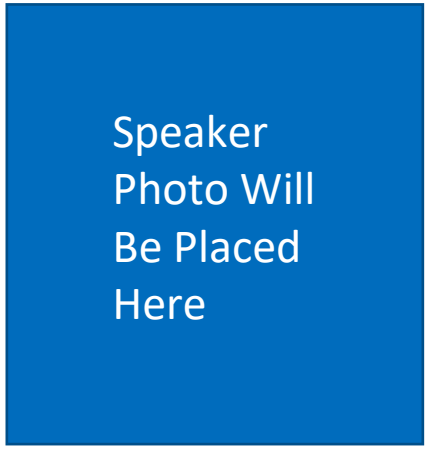
Xilinx
University of Cambridge

Source for Some Perspectives:

7 Things I learned from the IEEE Hot Interconnects Panel on SmartNICs

Technology Evangelist



7. Software today shapes hardware tomorrow
6. DPUs are evolving into computational storage controllers
5. Side Channel Attacks are a consideration
4. Cross pollination is happening
3. Monterey may be the data center OS
2. The CPU on the DPU is fungible
1. SmartNIC chiplet adoption may pivot on direct connect photonics

Architecture: Von Neumann

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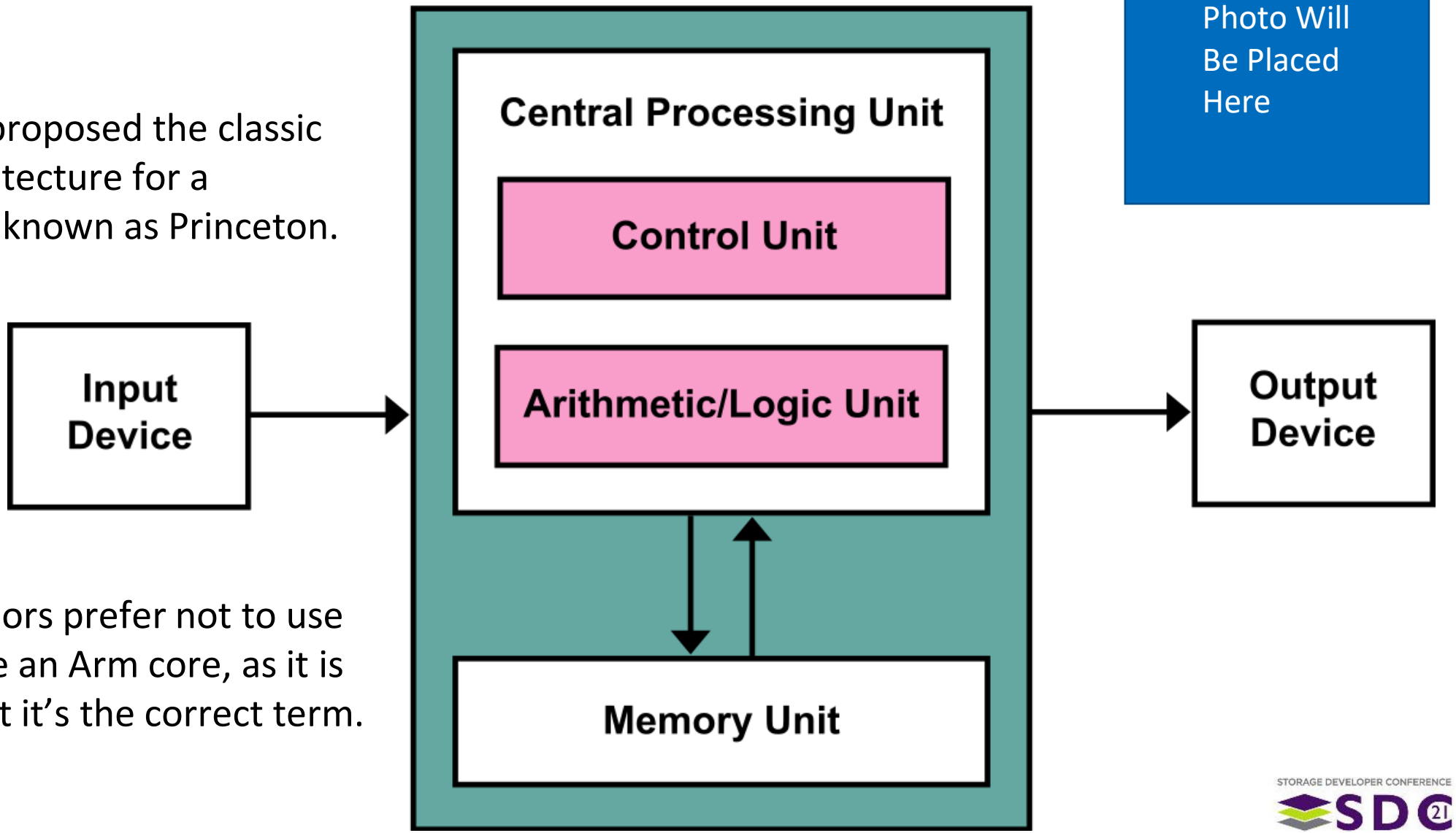
John Von Neumann proposed the classic stored program architecture for a CPU back in 1945, as known as Princeton.



Some SmartNIC vendors prefer not to use this name to describe an Arm core, as it is over 75 years old, but it's the correct term.

Architecture: SmartNIC/DPU/IPU/DSC

The VMWare Project Monterey Definition

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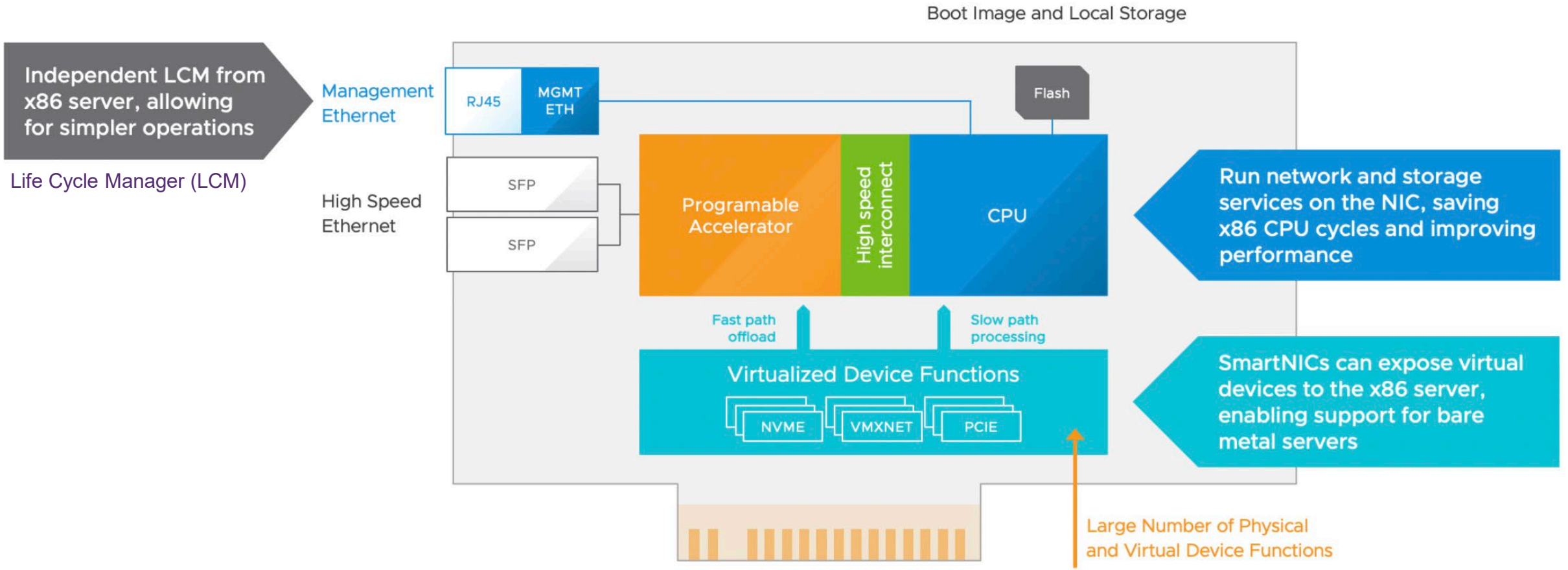

The Players: The Big Three

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- All have leadership in one or more critical markets
- Gargantuan economies of scale, in all areas
- Massive hard IP libraries & acquisition capability to expand
- Considerable software platforms

The Players:

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- Leadership in GPUs, Networking (Ethernet & Infiniband)
- Already announced cross pollination efforts with:
  - BlueField 2X, 3X and 4 roadmap
- Considerable software across all platforms
  - Their CUDA API for GPGPU defined the industry

The Players:

Speaker Photo Will Be Placed Here

- They invented the microprocessor!
- They have it all: CPUs, GPUs, FPGAs, and software
- Cross pollination of x86 into SmartNICs is has started to happen
- Their compiler technology is second only to IBM's
  - Could be the only vendor to deliver a hybrid compiler
- Platform software integration has always been a weak point

The Players:

Speaker Photo Will Be Placed Here

- CPU leader, #2 in GPUs, now adding FPGAs
  - Special class accelerators: SmartNICs, AI/ML, video, crypto mining
- Expect extensive cross pollination: IP blocks, software & chiplets
  - Could extend existing GPU software platform to include FPGAs
- Not a Monterey player, yet

The Players: Achronix MARVELL PENSANDO

Speaker Photo Will Be Placed Here

- Achronix, #3 FPGA, only independent, new 7nm platform
- Marvell, significant in size, but lacks breadth of big three
- Startup focused on distributed services card (DSC)
  - VMWare Monterey participant
  - Pushing server OEMs, like Lenovo, to be adopted

The Market Place is the Battle Field

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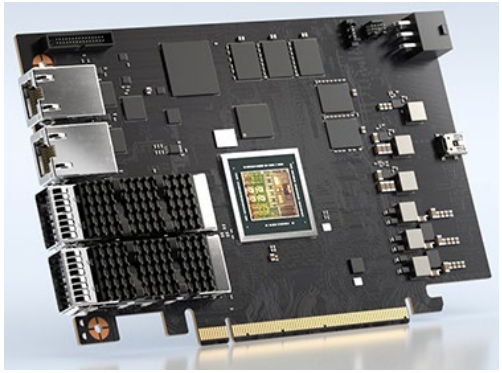
Von Neumann

Marvell - Octeon TX2



NVIDIA - BlueField 2

Pensando Naples

MARVELL
NVIDIA
PENSANDO
Achronix
intel
XILINX

Programmable Logic

Achronix/Bittware S7t-VG6

Intel C5020X & N5010

Xilinx Alveo SN1000 & U50

Software Today, Hardware Tomorrow

- Tools to convert programs for Arm & GPUs into gates
  - Optimized, trusted and proven routines into IP blocks
  - High level synthesis tools for converting C, C++ & CUDA
    - Easier to use
    - More pervasive

- VMWare Monterey has ESXi executing on an Arm core in the DPU
  - Provides for a security air gap from host ESXi instance
  - Enables ESXi to finally address “bare-metal” deployments

Software Today, Hardware Tomorrow

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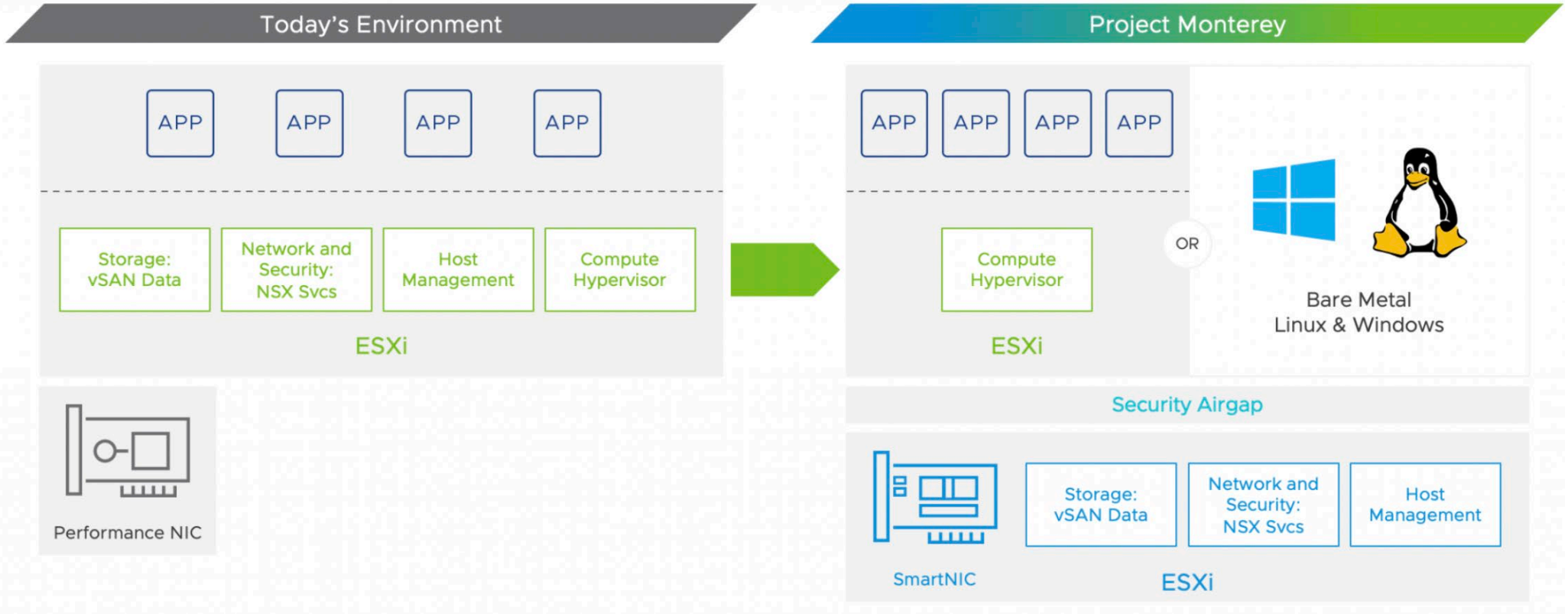

Additional Important Issues

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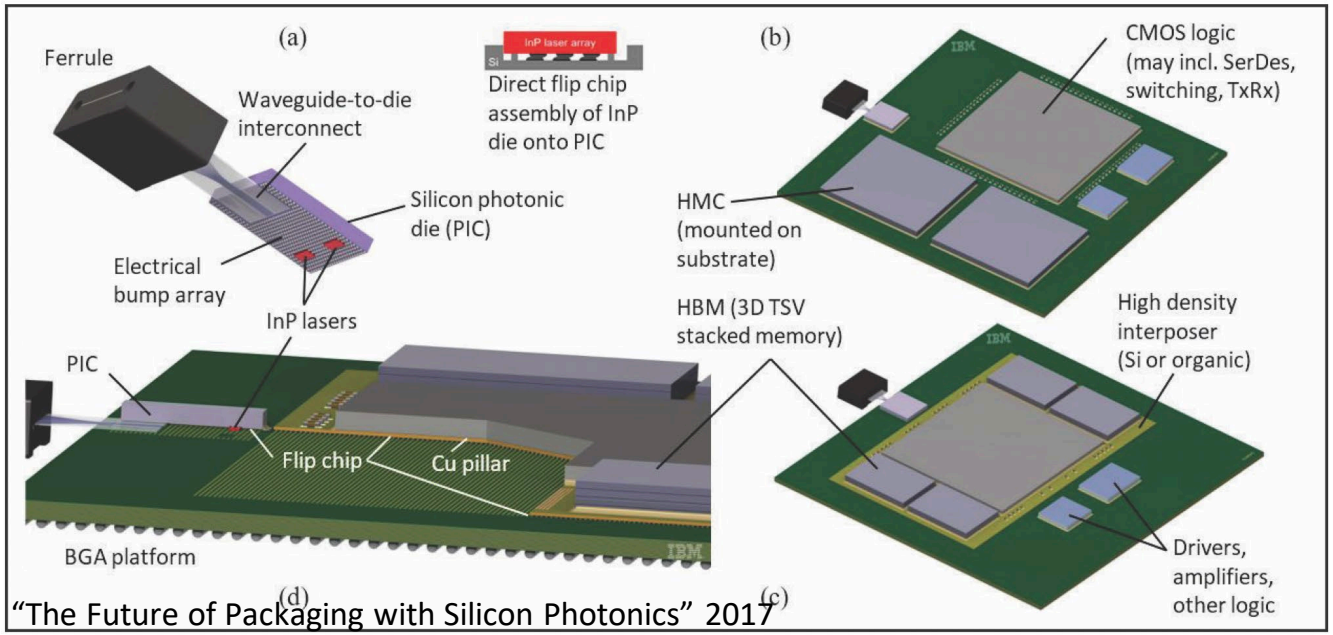
- Side Channel Attacks (SCA) are now a consideration
  - Power & Electromagnetic (EM)
  - Deploying counter measures often double gate counts

- DPUs will migrate enmass to chiplets when silicon photonic dies with waveguide-to-die or laser-to-die are brought right into the package



"The Future of Packaging with Silicon Photonics" 2017

Summary

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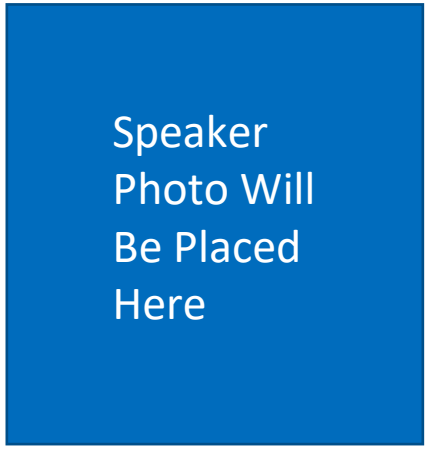
- Arm may have won
  - Monterey may drive at least one Arm core into SmartNICs for control plane
  - Eventually Monterey may be the OS of the DC, but its not fait accompli
    - Opportunity for open-source to compete is now
      - Across CPUs: RISC-V & x86 (Intel & AMD)
      - This may become critical if NVIDIA/Arm merger is approved
- Expect NVIDIA to add Arm packet processing instructions to internal DPU instances
- Frequently used code will become IP blocks on future chips
- SCA are worthy of consideration when designing DPUs
- Packaging chiplets will take over when silicon photonics-die mastered

So Who Won?



- Like most tech purchases, SmartNICs are rapidly evolving
- Today Monterey is poised to dominate, but tomorrow…
- Arm will be everywhere, but eventually could be almost nowhere
- Programmable logic will be more pervasive, and eventually a chiplet
- So who wins, the consumer!

Thank You

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